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A Study on Electrical and Material Characteristics of Hafnium Oxide with Silicon Interface Passivation on III-V substrate for Future Scaled CMOS Technology

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A Study on Electrical and Material Characteristics of Hafnium Oxide with Silicon Interface Passivation on III-V substrate for Future Scaled CMOS Technology

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Dedicated to

My wife, Hyunju Lim, my parents, and my parents-in-law, who have been my strong supporters, Chi Up Ok, Jung Ja Son, Young Hwan Lim and Young Ja Kim

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A Study on Electrical and Material Characteristics of Hafnium Oxide with Silicon Interface Passivation on III-V substrate for Future Scaled CMOS Technology

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The continuous improvement in the semiconductor industry has been successfully achieved by the reducing dimensions of CMOS (complementary metal oxide semiconductor) technology. For the last four decades, the scaling down of physical thickness of SiO_2 gate dielectrics has improved the speed of output drive current by shrinking of transistor area in front-end-process of integrated circuits. A higher number of transistors on chip resulting in faster speed and lower cost can be allowable by the scaling down and these fruitful achievements have been mainly made by the thinning thickness of one key component - Gate Dielectric - at Si based MOSFET (metal-oxide-semiconductor field effect transistor) devices. So far, SiO_2 (silicon dioxide) gate dielectric having

the excellent material and electrical properties such as good interface (i.e., D_{it} ~ $2x10^{10}$ $eV^{-1}cm^{-2}$), low gate leakage current, higher dielectric breakdown immunity (≥10MV/cm) and excellent thermal stability at typical Si processing temperature has been popularly used as the leading gate oxide material.

The next generation Si based MOSFETs will require more aggressive gate oxide scaling to meet the required specifications. Since high-k dielectrics provide the same capacitance with a thicker film, the leakage current reduction, therefore, less the standby power consumption is one of the huge advantages. Also, it is easier to fabricate during the process because the control of film thickness is still not in the critical range compared to the same leakage current characteristic of SiO_2 film. HfO_2 based gate dielectric is considered as the most promising candidate among materials being studied since it shows good characteristics with conventional Si technology and good device performance has been reported. However, it has still many problems like insufficient thermals stability on silicon such as low crystallization temperature, low k interfacial regrowth, charge trapping and so on. The integration of hafnium based high-k dielectric into CMOS technology is also limited by major issues such as degraded channel mobility and charge trapping. One approach to overcome these obstacles is using alternative substrate materials such as SiGe, GaAs, InGaAs, and InP to improve channel mobility.

The advantages of high electron mobility of III-V have long been recognized, and many efforts to fabricate MOS transistors have been pursued. The key challenge for III-V-based metal-oxide-semiconductor field effect transistor (MOSFET) is the lack of high-quality, thermodynamically stable insulators that passivate the interface states and prevents Fermi level pinning at III-V-gate dielectric interface.

In the first part of this study, several approaches to develop and understand the electrical characteristics of TaN/HfO_2/GaAs MOS capacitors with Si interface passivation layer (IPL) under various PDA (post-deposition anneal) condition and various PVD Si deposition temperature/time will be described. Depletion mode transistor and self-aligned n- and p-channel GaAs MOSFETs using HfO_2 and silicon IPL with the results of plausible characteristics will be presented. Also, a new approach of high-k era on GaAs, which results in significantly improvement in electrical and material aspects for future CMOS technology, will be demonstrated.

As for second part of this study, for indium based substrate application, material and electrical characteristics of self-aligned n-MOSFET with PVD Si IPL under various post deposition anneal (PDA) conditions on InGaAs and InP has been proposed and investigated. We also demonstrated N-channel high-k InGaAs and InP MOSFETs with good transistor behavior.

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Chapter 1: Introduction

1.1 CHALLENGES FOR GATE OXIDE SCALING

Over the last more than four decades, a successful evolution of Si-based semiconductor technology to increase circuit functionality and performance at lower cost has been continuously driven by scaling down of the metal-oxide-semiconductor field effect transistor (MOSFET). The Semiconductor Industry Association (SIA) has evaluated the goal of industry's products and established a "roadmap" since 1992 to predict the future performance demands and expectations of devices. The roadmap generally considers device capabilities, incorporated materials, design criteria, and the industries associated hardware. Based on the most recent roadmap as shown in Table 1.1, certain performance goals in near future appear simply unachievable for given the current compliment of materials and technologies. A continuous scaling-down of the MOSFET device with the minimum feature size of 23 nm and below requires EOT (Equivalent Oxide Thickness) less than ~ 9 Å. So far, SiO_2 gate dielectric has been popularly used as the leading gate oxide material in the field-effect transistor due to good interface (i.e., D_{it} ~ $2x10^{10}$ $eV^{-1}cm^{-2}$), low gate leakage current, higher dielectric breakdown immunity (≥ 10 MV/cm) and excellent thermal stability at typical Si processing temperature. However, as the dramatic scaling-down is continuously needed, ultra-thin silicon dioxide cannot be allowable any more as a gate dielectric since the use of ultra-thin SiO_2 gate dielectrics gives rise to a number of problems, including high gate leakage current, reduced drive

current, reliability degradation, boron (B) penetration, and the need to grow ultra thin and uniform layer. Main limitation for gate oxide scaling based on SiO_2 is huge direct tunneling current since the tunneling current increases exponentially with decreasing physical thickness of SiO_2. Increased leakage current can degrade standby-power dissipation and DRAM retention time, add to SRAM power consumption, offset of SRAM beta-ratio, reduce noise margin for CMOS inverter, which is basic component in CMOS logic, and accelerate device degradation [1, 2]. Because each device application determines allowable power consumption due to gate leakage current, requirement of gate leakage current for low power application is much stricter rather than that of high performance.

	Production Year	2007	2008	2009	2010	2011	2012
MPU /ASIC	Minimum Feature Size (nm)	25	23	20	18	16	14
	EOT (nm)		0.9	0.75	0.65	0.55	0.5
	Gate dielectric Leakage at 100 ºC (A/cm^2)	8.0E2	8.7E2	1.0E3	1.1E3	1.3E3	1.4E3
	S/D Junction Depth (Xj, nm)	27.5	25.3	19.8	17.6	15.4	

Table 1.1 Minimum feature size and EOT for high-speed devices (i.e. MPU) (from 2007 ITRS roadmap [3])

In addition, a SiO_2 layer of 10~15Å corresponds to only around 3~4 monolayers, which will be big concern for thickness uniformity across 300mm wafer for mass production in a next few years. Thus, the many alternate gate dielectric materials with high dielectric constant (> 3.9) have been emerging to replace conventional SiO_2 gate

dielectric because these materials can prevent the direct tunneling with fairly high thickness while maintaining same capacitance as like SiO_2 [4]. Therefore, higher dielectric constant material, so-called "high-k" gate dielectrics, with physically thicker material have been investigated. It can achieve larger oxide capacitance, but reduce gate leakage due to physically thick film while keeping same required capacitance following eq. 1.2 [4]

1.2 HIGH-K GATE DIELECTRICS: ALTERNATIVE MATERIAL FOR SILICON-BASED TRANSISTORS

High-k gate dielectrics have been studied as alternative gate dielectrics for the 70 nm technology node and beyond to replace conventional SiO_2 or silicon oxynitrides (SiO_xN_y). Principal requirements for high-k dielectric applications are 1) high dielectric constant 2) high band offset with electrodes (i.e. barrier height) to suppress leakage current 3) thermally and chemically stable in contact with Si substrate. Among these materials, HfO_2 has been shown to be compatible with poly-silicon gate [5, 6], poly-SiGe [7], and TaN gates [8]. In contrast, ZrO_2 has been reported that it was not compatible with poly-Si gate due to the reaction of Zr with poly-Si gate [9]. MOSFETs with HfO_2 dielectrics and TaN gate showed very low EOT (~10-12Å) and low leakage current even after the conventional CMOS process flow [8]. Considering the cost of development and implementation, HfO_2 gate dielectric needs to span two or three generations from the 75 nm to the 35 nm design rule. To meet the requirements for these generations, EOT should be scaled down to less than 10 Å while suppressing leakage current to below 1 A/cm^2

[10]. Currently Hf based material has been extensively investigated in order to overcome the intrinsic disadvantages of HfO_2 such as lower crystallization temperature, formation of interfacial oxide layer with Si substrate, low channel mobility, etc. Optimization of annealing condition with forming gas or deuterium has demonstrated the improvement of electrical characteristics, particularly channel electron mobility [11, 12]. However, there are still lots of issues to be concerned. Due to the significant preexisting traps and fast transient charge trapping/detrapping, it is not easy to understand the electrical characteristics of high-k device using the conventional characterization technique for SiO_2 based devices [13, 14, 15, 16]. Reduced transistor performance in high-k dielectric such as reduced carrier mobility, saturation current, and hysteresis was addressed that trapped charges during the conventional measurement were the primary reason. These trapped charges have very small time constant. Therefore, these easily jump up to the trap sites in dielectric layer and go back to substrate during very short characterization time. To characterize these transient charges, transient measurement technique has been proposed for high-k devices [17, 18, 19, 20, 21]. For mobility characterization, the most important parameter is inversion charge density. The electron mobility was usually calculated from drain current-gate bias (I_d-V_g) curve and gate to channel capacitance (C_{gc}) vs. V_g curves (not shown here) of the MOSFETs using a well-known equations (1.1) [22]. Effective mobility of carrier can be expressed by a simple equation (1.1),

$$\mu_{eff}(V_g) = \frac{I_d / V_d}{(W / L) Q_{inv}(V_g)} \qquad (1.1)$$

One approach to overcome mobility degradation is using compound semiconductors. Compound semiconductors have the potential to rival Si CMOS devices in areas such as high-performance CMOS and hi-temperature, high-power, high-frequency electronics.

1.3 COMPOUND SEMICONDUCTORS MOS FOR HIGH PERFORMANCE DIGITAL TECHNOLOGY

As reported in ITRS, improvements in the transistor drive current can be achieved by enhancing the average velocity of carriers in the channel, in addition to other approaches such as multi-gate MOSFET, carbon nano-tube FET, resonant tunneling FET, single electron transistor, and molecular devices. Approaches to enhancing carrier velocities include mechanically straining the channel layer to enhance carrier mobility and saturation velocity, and employing alternative channel materials such as silicon-germanium, germanium, and III-V and lower effective masses than those in silicon.

MOSFETs made of GaAs, which has an electron mobility that is about 4 times as high as that of Si, a similar saturation velocity as that of Si, and a band-gap energy that is 1.3 times as high as that of Si, allows improved on-state drive current (I_{ON}) without increasing the off-state leakage current (I_{off}); while MOSFETs made of some other alternative channel materials, such as Ge, InAs, and InSb may pay the price of higher I_{off}, due to their smaller band-gap energies. So, GaAs is a better candidate for CMOS technology in this sense.

In the late 1920's, the scientific community's attention turned to gallium arsenide (GaAs) as another material with semiconductor properties. As time progressed, however, it was noticed that there were numerous barriers to the development and ultimate use of GaAs as a practical alternative to other existing device materials like germanium and more prominently later, silicon. The absence of technology to generate device grade GaAs was one such hurdle. Initial enthusiasm died down, only to be revived later by technological advances in manufacturing processes. Such breakthroughs have helped bring GaAs out from experimental labs to the commercial market and regenerate debates about it as a silicon substitute. However, very small amount of the integrated circuit (IC) market is controlled by GaAs devices and the figure is not likely to go up till more of the complex issues involving GaAs are resolved.

Since the first demonstration of a depletion-mode GaAs MOSFET in 1965 [23], GaAs has been regarded as a "semiconductor of the future", and intensive research for enhancement-mode MOSFET has been continuously carried out. Enhancement-mode MOSFET is favored because it is a 'normally-off' device, meaning when there is no gate bias applied, the channel is off, and this greatly reduces the standby power of devices and circuits. An enhancement-mode MOSFET relies on semiconductor surface in version to turn on.

Recently, only one dielectric have made unequivocal demonstrations of GaAs enhancement-mode transistor, which includes Ga_2O_3 and its derivatives [24], while GaAs surface inversion has also been demonstrated with Al_2O_3 as a gate dielectric

[25]. The inability to unpin the GaAs surface Fermi level and form a GaAs surface inversion layer has largely hindered the progress in this field in the last forty years.

However, a great deal of surface and interface physics and chemistry of GaAs and dielectric/GaAs system have been investigated in research. It has been found that, due to surface oxygen chemisorption, interfacial lattice defects, and stoichiometry perturbation, high interface-state densities (between 10^{12}~10^{14} /$cm^{-2}eV^{-1}$) between GaAs and dielectrics and GaAs surface pinning have been commonly observed throughout the literature. Various models have been proposed to explain such phenomena, such as "Unified defect model' by Spicer; "Misfit dislocation model" by Woodall, and "unified disorder induced gap state model" by Hasegawa [26, 27, 28].

Our group has demonstrated device-quality PVD (physical vapor deposition) SiO_2/Si/GaAs system, which rivals high quality SiO_2/Si system with low interface defect density and high electron mobility. So, this research studies the feasibility of PVD SiO_2/Si on GaAs for MOS device technology.

1.4 OUTLINE

Electrical properties of Hf-based high-k dielectric materials on compound semiconductor such as GaAs, InGaAs and InP in this study are based on understanding of physics, reliability, and process development in MOSCAP and MOSFET characteristics.

Chapter 2 covers several approaches to develop and understanding the electrical characteristics of TaN/HfO_2/GaAs MOS capacitors with Si IPL under various PDA (post-

deposition anneal) condition and various PVD Si deposition temperature/time will be described. The insertion of the ultra thin Si layer is designed to establish one-to-one registry between the semiconductor and the insulator and also, in the case of SiO_2, prevents the GaAs from oxidation. Depletion mode transistor and self-aligned n- and p-channel GaAs MOSFETs using HfO_2 and silicon IPL with the results of plausible characteristics will be presented. Also, a new approach of high-k era on GaAs, which results in significantly improvement in electrical and material aspects for future CMOS technology, will be demonstrated.

Chapter 3 presents the investigation $In_{0.2}Ga_{0.8}As$ MOSCAP using the same oxide of HfO_2 as gate insulator with Si IPL. In this chapter, we present $In_{0.2}Ga_{0.8}As$ MOSCAP using the same oxide of HfO_2 as gate insulator with Si IPL using physical vapor deposition (PVD) sputtering system. We studied the electrical characteristics of TaN/HfO2/GaAs MOS capacitors with Si IPL under various PDA (post-deposition anneal) condition and various Si deposition time using MBE grown $In_{0.2}Ga_{0.8}As$ substrate. . Also, we have investigated hydrogen incorporation effects for $In_{0.2}Ga_{0.8}As$ MOSCAP using the same structure and H_2 annealing.

We present metal-oxide-semiconductor capacitor (MOSCAP) using the same oxide of HfO_2 by PVD as gate insulator without Si IPL but on high-indium-content $In_{0.53}Ga_{0.47}As$ channel. We report the electrical characteristics of $TaN/HfO_2/In_{0.53}Ga_{0.47}As$ MOS capacitors under various PDA (post-deposition anneal) condition and various indium content on InGaAs substrate. MOS capacitors were fabricated on molecular beam epitaxy (MBE) grown n-type $In_{0.53}Ga_{0.47}As$ wafers doped with Si on n-type InP substrate. Also, we presents the electrical characteristics of $TaN/HfO_2/In_{0.53}Ga_{0.47}As$ MOS

capacitors under various PDA (post-deposition anneal) condition and self-aligned n-channel MOS transistor with high temperature PMA on high-indium-content $In_{0.53}Ga_{0.47}As$ channel substrate.

Chapter 4 explains the details of process development in InP substrate with HfO_2 and Si IPL for future CMOS technology. In this work, as an alternative of silicon substrate, InP has been studied. We present the material and electrical characteristics of $TaN/HfO_2/InP$ MOS capacitors and self-aligned n-MOSFET with PVD Si IPL under various post deposition anneal (PDA) conditions and PMA. We also demonstrated N-channel high-k InP MOSFETs with good transistor behavior.

Finally, chapter 5 summarizes the studies above and suggests the possible future researches in this area.

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Chapter 2: MOSCAP's and MOSFET's on GaAs Channel Materials with Si, SiGe Interface Passivation Layer

2.1 DEVELOPMENT OF PROCESS FABRICATION: SI IPL ON GAAS

2.1.1 Motivation

The motivation for this work is to explore and develop high-k dielectrics on GaAs. High-k dielectrics, such as HfO_2, have been considered as alternative to SiO_2 in Si-based CMOS technology. The alternative dielectrics provide excellent opportunity for considering alternative channel materials such as SiGe [1-2]. Alternative substrates such as InAs and InSb with very high carrier (here is electron.) mobility also are important to fabricate low-voltage and low power digital logic applications [3]. Among high mobility material candidates, very high mobility materials like InAs and InSb, have a much smaller direct band gap which gives rise to high band-to-band tunneling (BTBT) leakage (Fig. 2.1).

	Si	Ge	GaAs	InGaAs	GaN	InAs	InSb
Energy gap (eV)	1.12	0.66	1.43	0.75	3.4	0.305	0.17
Lattice constant (Å)	5.431	5.646	5.65	5.87	3.19	6.06	6.5
Electron effective mass	0.19	0.082	0.063	0.041	0.2	0.023	0.014
Electron mobility ($cm^2V^{-1}s^{-1}$)	1500	3900	8500	14000	1300	25000	78000

Table 2.1. Properties of important semiconductors

Smaller effective mass materials which have smaller bandgap materials have larger BTBT and larger off state current. And, the lack of a proper oxide material, high interface state density and being unstable with high temperature annealing make it very difficult to fabricate a good MOSFET on them at this moment. Even though the elusive GaAs-insulator interface with high quality is still one of the objectives for enhanced GaAs devices, GaAs has quite high electron mobility and good thermal stability with high band gap.

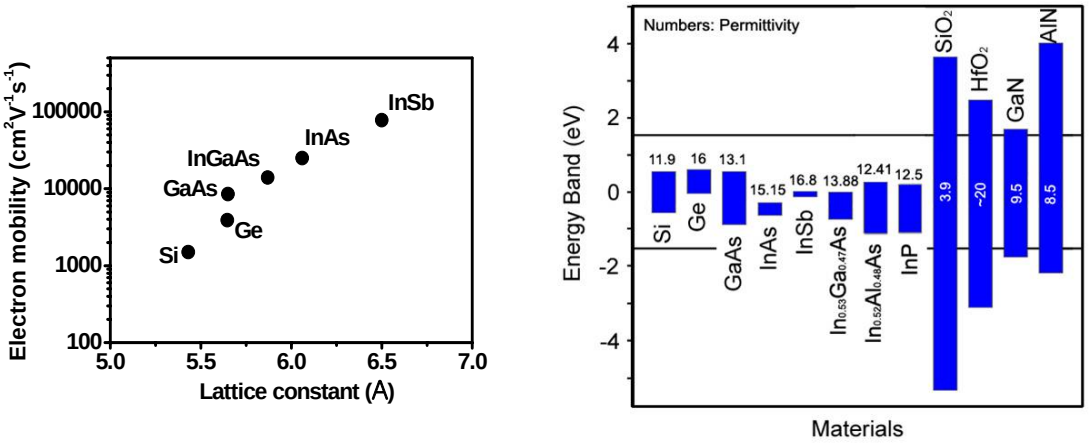

Figure 2.1. Electron mobility and energy band gap related between lattice and carrier mobility, through effective mass and materials

The advantages of the large band gap and high electron mobility of GaAs have long been recognized, and many efforts to fabricate MOS transistors have been pursued. Recent advances have yielded promising results for device application; for example, MOSFETs have been demonstrated using InAlP native oxide [4], gate insulators of Ga_2O_3 grown by molecular beam epitaxy (MBE) [5], oxidized GaAs prepared by ultraviolet and ozone treatment [6], Al_2O_3 grown by atomic layer deposition [7], [8], and wet thermally oxidized AlAs [9], [10].

Most of the previous research has focused on passivation of GaAs surface in order to "unpin" surface Fermi Level because a high surface state density can cause surface Fermi level pinning near the midgap in GaAs [3] (Fig. 2.2). To this end, Si_3N_4/Si/GaAs and SiO_2/Si/GaAs structures have been studied extensively [11-22]. Including Si interface passivation layers (IPL) [17-22], sulfur compounds [23], and surface cleaning using hydrogen or nitrogen plasma [21] also used for passivation techniques. Among these techniques, both the sulfide and silicon IPL passivation seem to be the most effective in order to "unpin" surface Fermi Level [17-24]. While these surface treatments did produce improved surface properties, the research thus far, however, has not identified an effective approach to achieve a high quality interface comparable to SiO_2/Si system. To make SiO_2/Si on GaAs, we used physical vapor deposition (PVD) Si IPL with $(NH_4)_2S$ (ammonium sulfide) treatment. The insertion of the ultra thin Si layer is designed to establish one-to-one registry between the semiconductor and the insulator and also, in the case of SiO_2, prevents the GaAs from oxidation. In our studies, the growth temperature of Si was 400°C-500°C to achieve the crystal quality of the Si layer which can be smoothed out only by adatom/adspecies surface migration at high temperatures using PVD system [25].

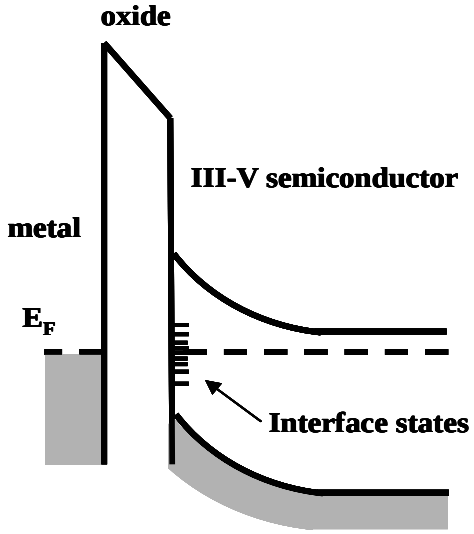

Figure 2.2. Fermi level pinning

In this chapter, several approaches to develop and understand the electrical characteristics of TaN/HfO_2/GaAs MOS capacitors with Si IPL under various PDA (post-

deposition anneal) condition and various PVD Si deposition temperature/time will be described. Depletion mode transistor and self-aligned n- and p-channel GaAs MOSFETs using HfO_2 and silicon IPL with the results of plausible characteristics will be presented. Also, a new approach of high-k era on GaAs, which results in significantly improvement in electrical and material aspects for future CMOS technology, will be demonstrated.

2.1.2 Experiments

MOS capacitors were fabricated on n-type GaAs (100) wafer doped with Si (1~5) e17. The surface oxides were removed with a HCl clean followed by $(NH_4)_2S$ dip, resulting in a clean S-passivated GaAs surface. Then Si IPL was deposited by RF sputtering of Si in Ar ambient at various temperatures (from 25°C - 500°C). PVD HfO_2 films were deposited using the modulation technique [26], followed by PDA at 600°C in N_2 (O_2 5%) ambient (Fig. 2.3).

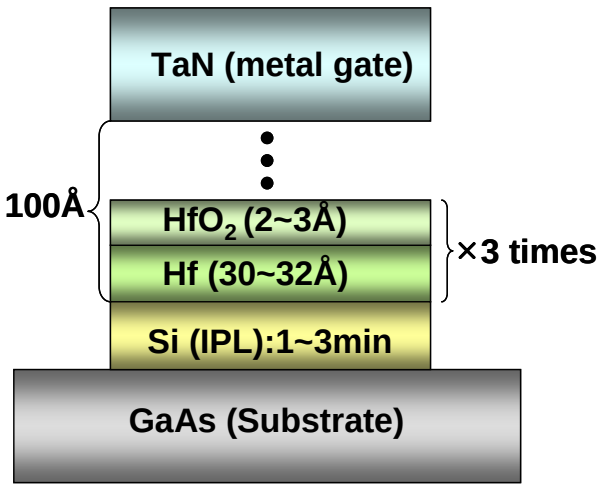

Figure 2.3. Layer structure of the Si-capped sample with Hf of 3 times modulation deposition.

The thickness of Si IPL layer varied from ~8Å (1min deposition time) to ~24Å (3min) ; and the physical thickness of HfO_2 layer was ~ 100Å. PVD TaN was used as gate electrode. After gate patterning using reactive ion etching (RIE) based on CF_4 gas, low-resistance ohmic contact was formed by using AuGe/Ni/Au alloy on the backside of the wafer [27]. The samples were then annealed at 450°C for 30sec in nitrogen. Electrical characterization was performed on MOS capacitors which were measured using HP4149A impedance analyzer with bias sweep rates 500mV/sec for C-V measurements and HP4156A parameter analyzer. Equivalent oxide thickness (EOT) values were extracted using a C-V simulation program. [28]

2.1.3 Characteristics of capacitor on n-type GaAs

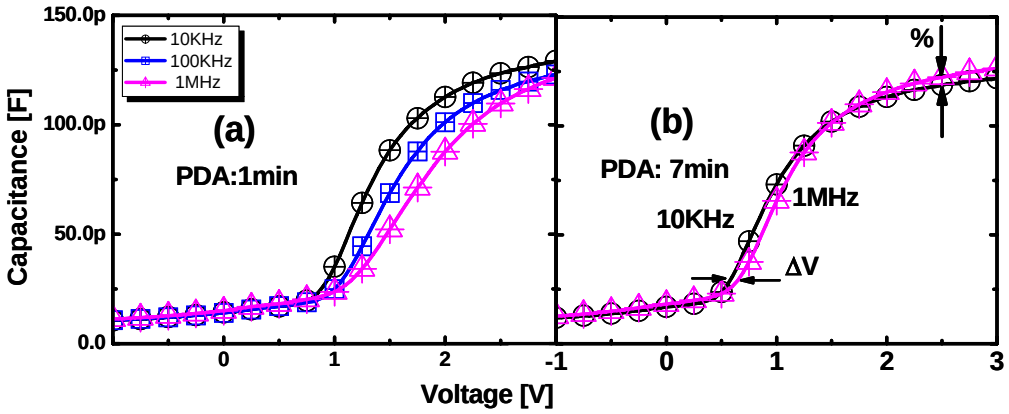

Figure 2.4. Typical C-V characteristics of $TaN/HfO_2/GaAs$ as a function of frequency for 1min Si IPL deposition time and varying PDA time: (a) 1min and (b) 7min.

Typical capacitance-voltage characteristics of TaN/HfO_2/GaAs as a function of frequency are shown in Fig 2.4. The samples consist of thin Si IPL layer thickness (with Si deposition time of 1min). It can be observed that well-behaved C-V characteristics have been obtained. Furthermore, the longer PDA time (Fig 2.4b) resulted in reduced frequency dispersion, relative to shorter PDA shown in Fig 2.4a. Fig. 2.5 summarizes the frequency dispersion characteristics (ΔV and % are defined in Fig 2.4b) versus PDA time as a function of Si IPL deposition condition. With Si capping layer, low frequency dispersion (< 5%) can be obtained. In contrast, without Si capping layer, frequency dispersion was around 25% (Fig 2.5b). In general, shorter Si deposition time (1min or 2min) and longer PDA time resulted in reduced frequency dispersion. It should be emphasized that these frequency dispersion values are very low reported in the literature [29]. The results suggest that there is negligible Fermi level pinning at the surface [30].

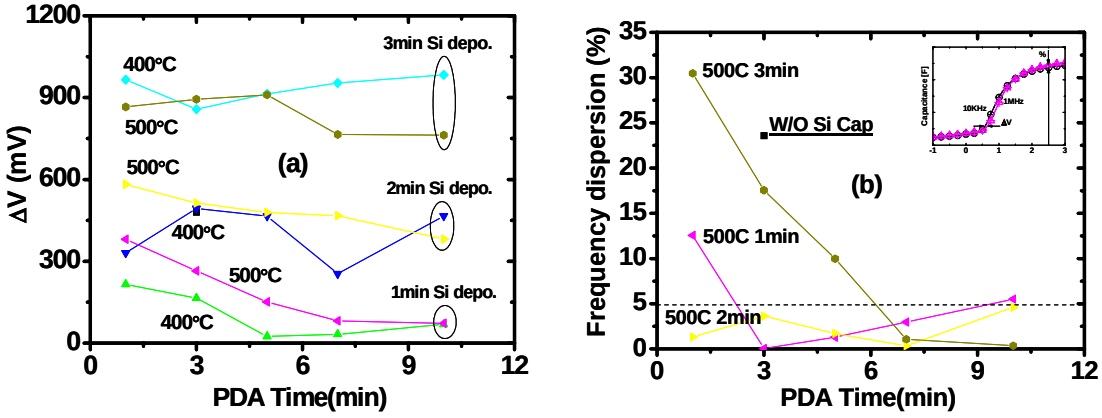

Figure 2.5. Frequency dispersion versus PDA time as a function of Si IPL deposition condition: (a) voltage difference (mV) at flat band voltage; and (b) capacitance difference (%) between 1MHz and 10KHz.

Shorter Si deposition time (thinner IPL) and longer PDA time generally resulted in sharper C-V curve (i.e. reduced interface state density) (Fig. 2.6a).

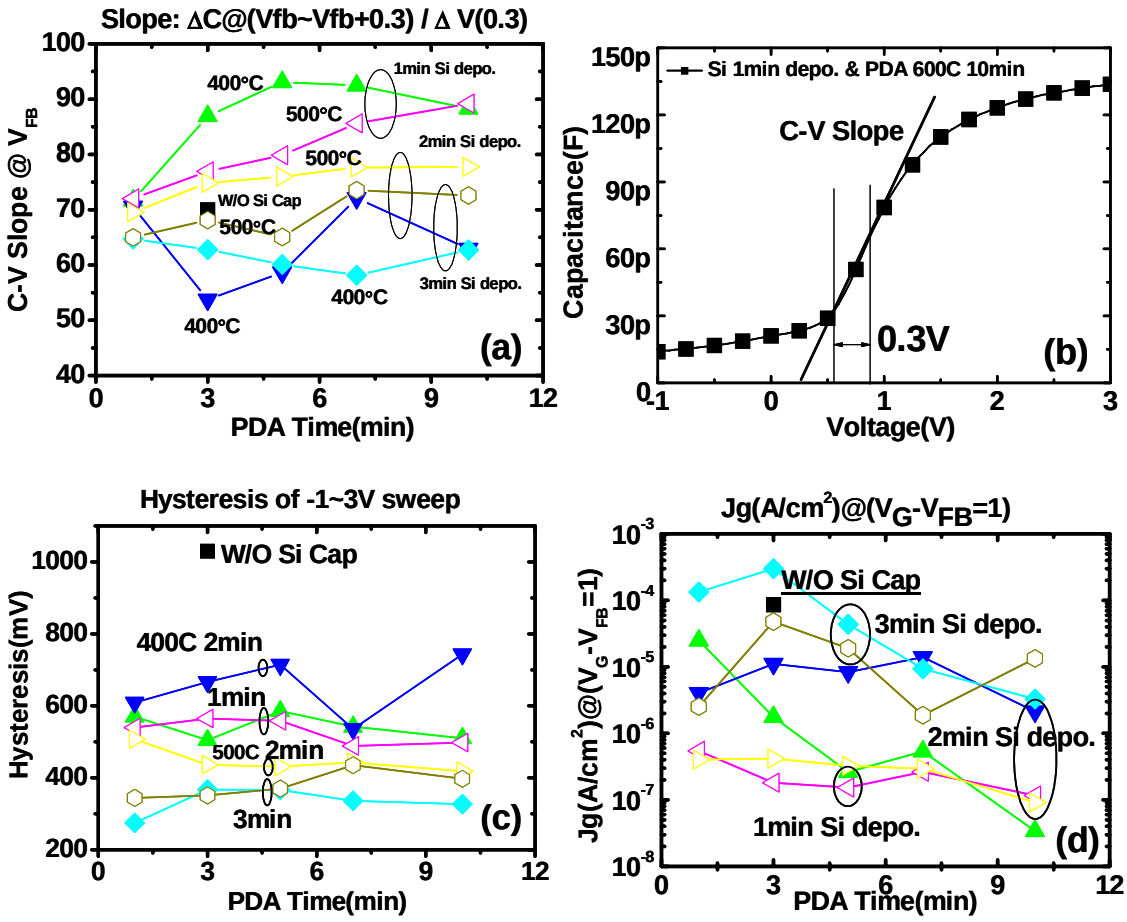

Figure 2.6. (a) C-V slope (b) definition of C-V slope (c) Hysteresis (d) Leakage current density versus PDA time as a function of Si IPL deposition condition.

The slope in C-V curve was extracted at V_{FB} to V_{FB}+0.3V (see Fig. 2.6b). Also, Si – capped (thin IPL) MOSCAP exhibited sharper C-V curves than non-Si capped devices. There is no clear dependence of C-V shape on Si deposition temperature. High-k dielectrics are known to exhibit hysteresis. It has been found that the hysteresis was

reduced significantly using the Si IPL (Fig. 2.6c). In general, longer Si deposition time led to lower hysteresis except for 400°C 2min of Si IPL. However, longer Si deposition time also resulted in more severe stretched-out C-V curve (Fig. 2.6a). As we decreased the HfO_2 thickness we have smaller hysteresis and increased PDA condition we have a little hysteresis improvement. So most hysteresis is coming from HfO_2 itself and second reason is from reasonable PDA condition. And also interface quality affects the hysteresis from comparing with and without Si IPL hysteresis result. Fig. 2.6 (d) shows the leakage current density at V_g-V_{FB}=1 as a function of PDA time. Leakage current was significantly reduced by using the Si IPL. In general, longer PDA time, shorter Si-deposition time and higher Si deposition temperature led to lower leakage current.

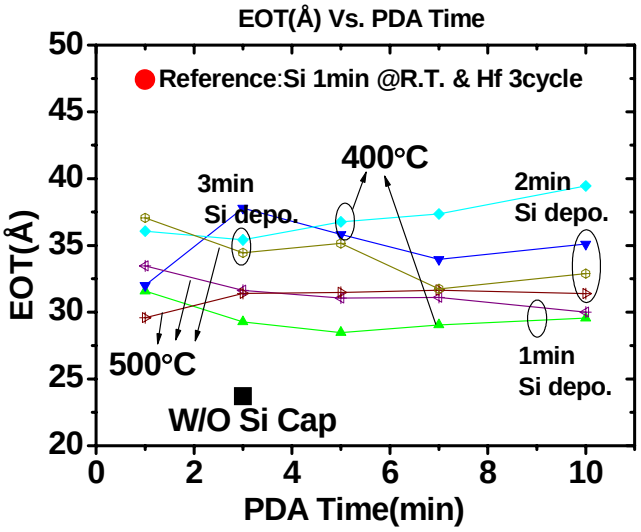

Figure 2.7. EOT versus PDA time as a function of Si IPL deposition condition with different Si IPL thickness and deposition temperature.

In general, shorter Si deposition time resulted in thinner EOT values. Note that the EOT value for thin Si IPL samples (1min Si deposition w/PDA time of 3-10min) was ~28.5Å –

29.5 Å. Even though EOT is thinner for sample W/O Si capacitor, C-V has severe stretch out, hysteresis and frequency dispersion. There are very thin EOT reported for GaAs MOSCAP (Fig. 2.7).

2.2 OPTIMIZATION OF SILICON IPL THICKNESS ON GAAS

2.2.1 MOSCAP characteristics on n-GaAs Substrate

TaN/HfO_2/GaAs MOS capacitors on n-type GaAs (100) wafer have been fabricated. Various deposition time (thicknesses) of Si IPL under various PDA (post-deposition anneal) condition have been used.

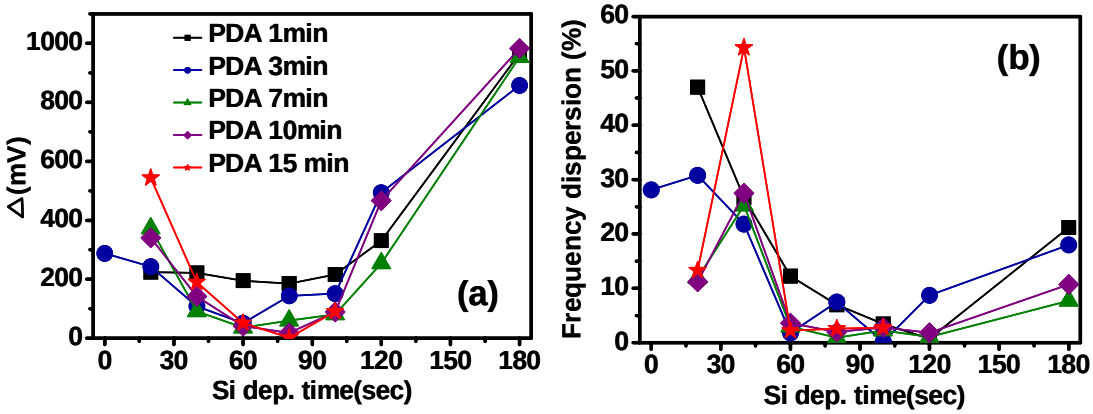

Figure 2.8. Frequency dispersion versus Si IPL deposition condition as a function of PDA time: (a) voltage difference (mV) at flat band voltage; and (b) capacitance difference (%) between 1MHz and 10KHz.

Fig. 2.8 summarizes the frequency dispersion characteristics versus Si IPL deposition condition as a function of PDA time. With appropriate thickness of Si capping layer, low

frequency dispersion (<50mV and < 5%) (Fig. 2.8) can be obtained. In contrast, without Si capping layer (0 Si deposition time) frequency dispersion was around ~300mV and 25%. In general, Si deposition time of ≈ 60-100 second and longer PDA time resulted in reduced frequency dispersion. Frequency dispersion is more depended on Si deposition time than on PDA condition. Si deposition time of ≈ 60-100 second and longer PDA time generally resulted in sharper C-V curve (i.e. reduced interface state density) (Fig. 2.9a).

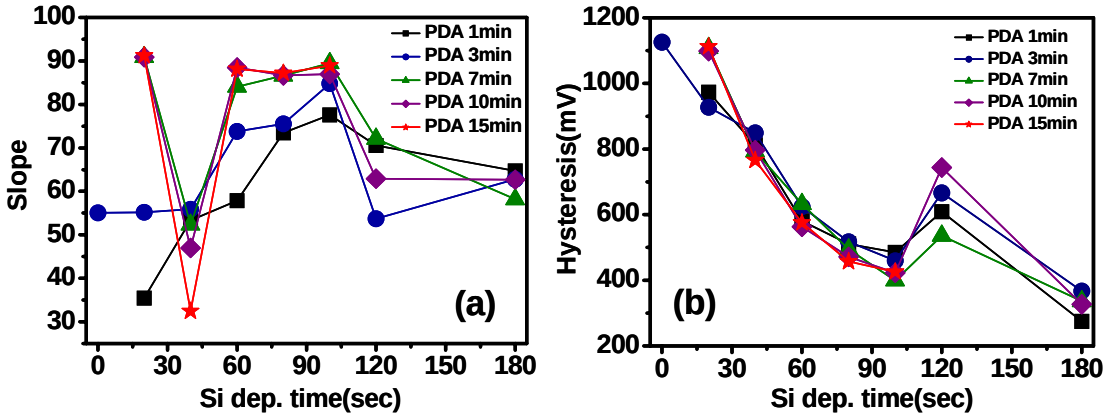

Figure 2.9. (a) C-V slope (b) hysteresis versus Si IPL deposition condition as a function of PDA time.

The slope in C-V curve was extracted at V_{FB} to V_{FB}+0.3V ((Capacitance @ V_{FB}+0.3V - Capacitance @ V_{FB})/0.3V). Also, Si – capped (60sec~100sec of IPL deposition) MOSCAP exhibited sharper C-V curves than non-Si capped devices. Note that even though the 20sec Si resulted in sharp C-V cruve, it also exhibited large frequency dispersion, large hysteresis and non-saturated C-V. C-V slope also more depended on Si deposition time than PDA condition. High-k dielectrics are known to exhibit hysteresis. It has been found that the hysteresis was reduced significantly using the Si IPL (Fig. 2.9b).

In general, longer Si deposition time led to lower hysteresis. However, Si deposition time of >2min resulted in more severe stretched-out C-V curve and have high frequency dispersion as discussed above. Fig. 2.10 shows the leakage current density at V_g-V_{FB}=1 as a function of Si deposition time (Fig. 2.10a) and PDA time (Fig. 2.10b).

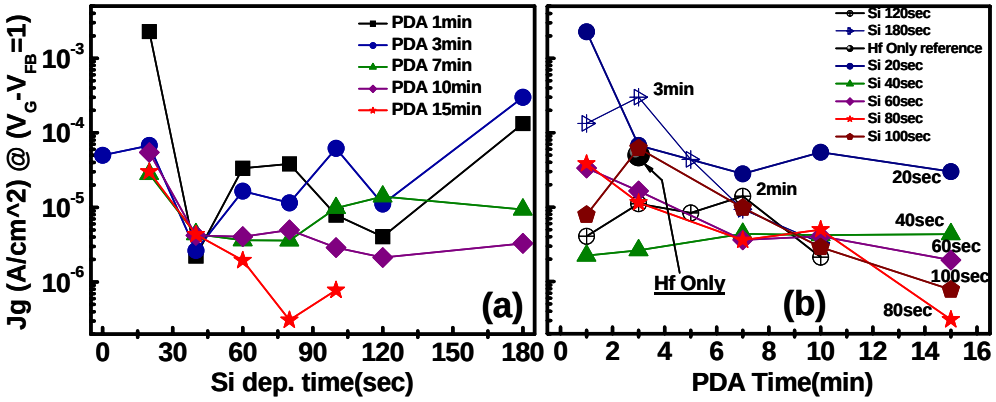

Figure 2.10. (a) leakage current density versus Si IPL deposition condition as a function of PDA time (b) Leakage current density versus PDA time as a function of Si IPL deposition condition.

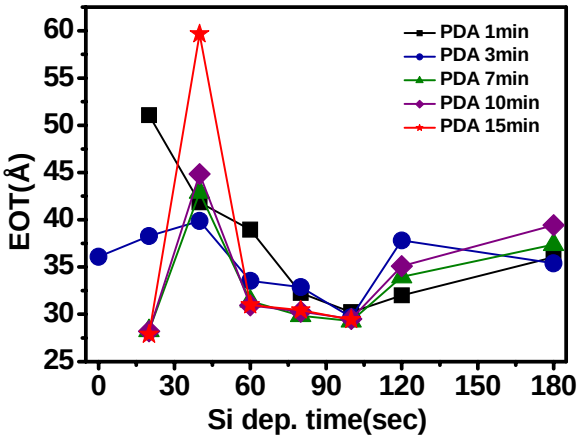

Figure 2.11. EOT versus Si IPL deposition time as a function of different PDA condition.

Leakage current was significantly reduced by using the Si IPL. In general, longer Si-deposition time at longer PDA time led to lower leakage current. Leakage current was found to be more depended on PDA condition than Si deposition time. In general, Si deposition time of 60sec~100sec resulted in thinner EOT values (Fig. 2.11). Note that even though EOT is thinner for sample 20 sec Si cap layer, C-V has severe stretch out, larger hysteresis and frequency dispersion

2.2.2 MOSCAP characteristics on p-GaAs Substrate

In this part, we have fabricated MOSCAPs on P-type GaAs using the same structure as n-type MOSCAPs. In general, frequency dispersion (ΔmV) was larger than those observed in N-type substrate capacitors in 60sec~100sec (Fig. 2.12a) and 60sec~120sec Si deposition time resulted in reduced frequency dispersion (< 5% in Fig 2.12a).

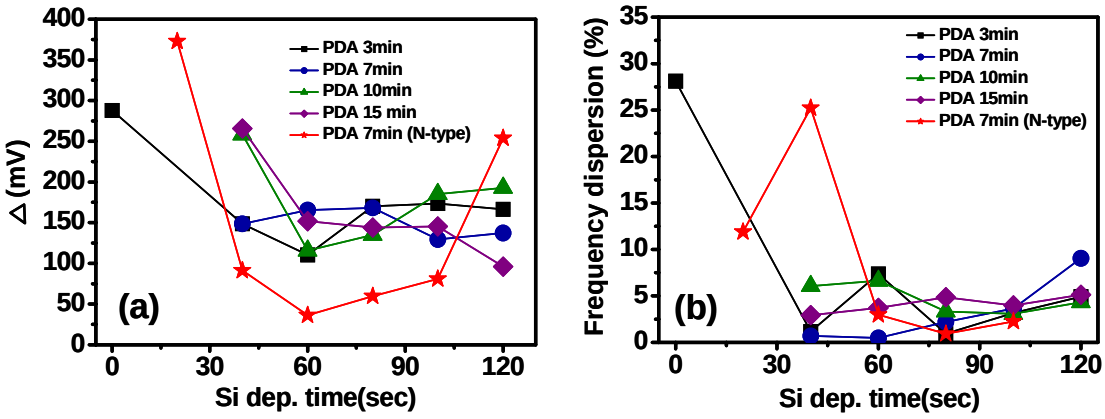

Figure 2.12. Frequency dispersion versus Si IPL deposition condition as a function of PDA time: (a) voltage difference (mV) at flat band voltage; and (b) capacitance difference (%) between 1MHz and 10KHz.

Si deposition time of 60sec~100sec generally led to sharper C-V curve (thus, possibly reduced D_{it}) in Fig 2.13a.

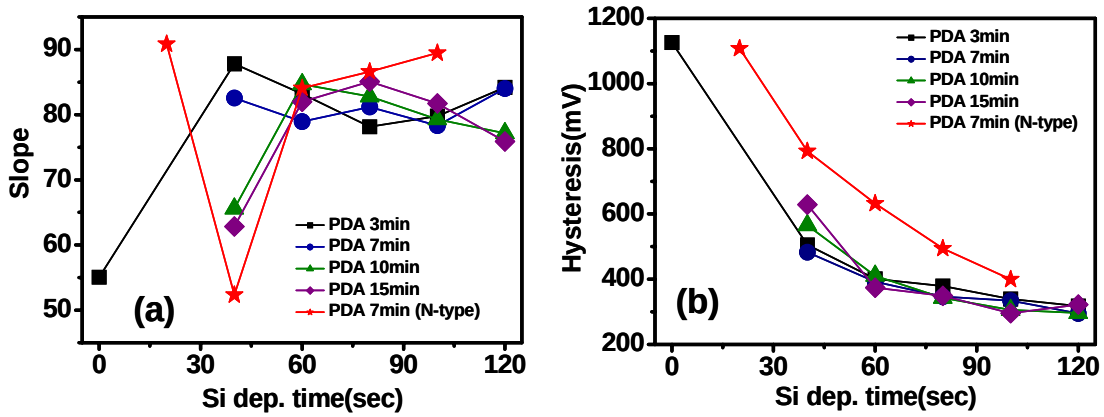

Figure 2.13. (a) C-V slope (b) hysteresis versus Si IPL deposition condition as a function of PDA time.

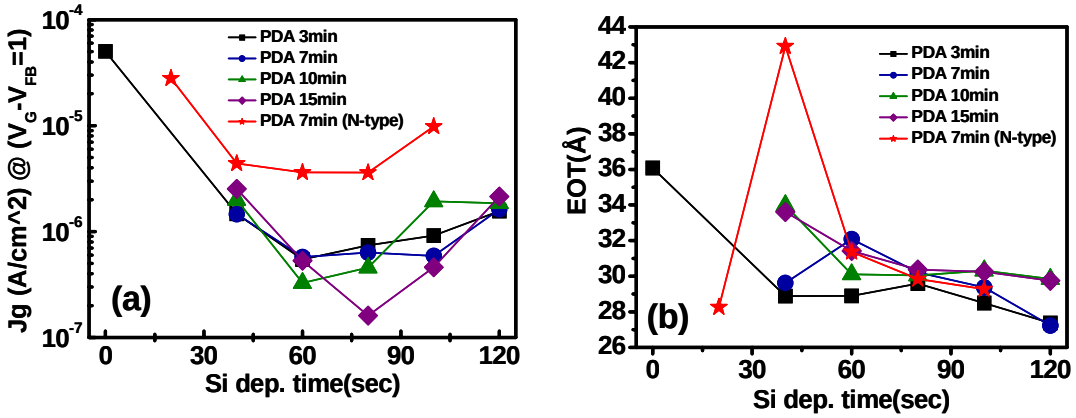

Figure 2.14. (a) leakage current density versus Si IPL deposition condition as a function of PDA time (b) EOT versus Si IPL deposition time as a function of different PDA condition.

Longer Si deposition time led to lower hysteresis. Generally, hysteresis observed in P-type MOSCAPs was lower than those on N-type substrate (Fig. 2.13b). Leakage current

was significantly reduced using the Si cap technique and longer PDA time resulted in lower J_L. Generally, leakage current observed in P-type MOSCAPs was lower than those on N-type substrate (Fig 2.14a). In general, longer Si deposition time resulted in thinner EOT values. Si IPL layer differences did not affect EOT thickness. Even though EOT is thinner for sample 120 sec Si cap layer, C-V has severe stretch out, leakage current, and frequency dispersion (Fig. 2.14b).

2.3 DEMONSTRATION OF DEPLETION MODE TRANSISTOR WITH MATERIAL AND ELECTRICAL ANALYSIS ON N-TYPE GAAS

2.3.1 MOSCAP characteristics on GaAs Substrate

We have demonstrated depletion mode MOSFET using optimum capacitance condition with material and electrical characteristics of TaN/HfO_2/GaAs MOS capacitors using Si IPL under various PDA (post-deposition anneal) condition and various Si deposition time. Excellent electrical characteristics with thin EOT (~2nm), low frequency dispersion (<5%) and high maximum mobility (568 cm^2/V-s) have been obtained.

Fig. 2.15a shows transmission electron microscopy (TEM) on the MOSCAP with 10nm HfO_2 with PDA of 600°C 3 min. The interface between HfO_2 and GaAs surface was degraded severely after 600°C 3 min PDA for sample without Si IPL. Electron energy loss spectroscopy (EELS) shows that Si was partially oxidized without PDA simply due to exposure to air after Hf deposition process (Fig. 2.15d). In Fig. 2.16 (a) shows Si IPL

protected the interface between HfO_2 and GaAs surface without degradation after 10min PDA.

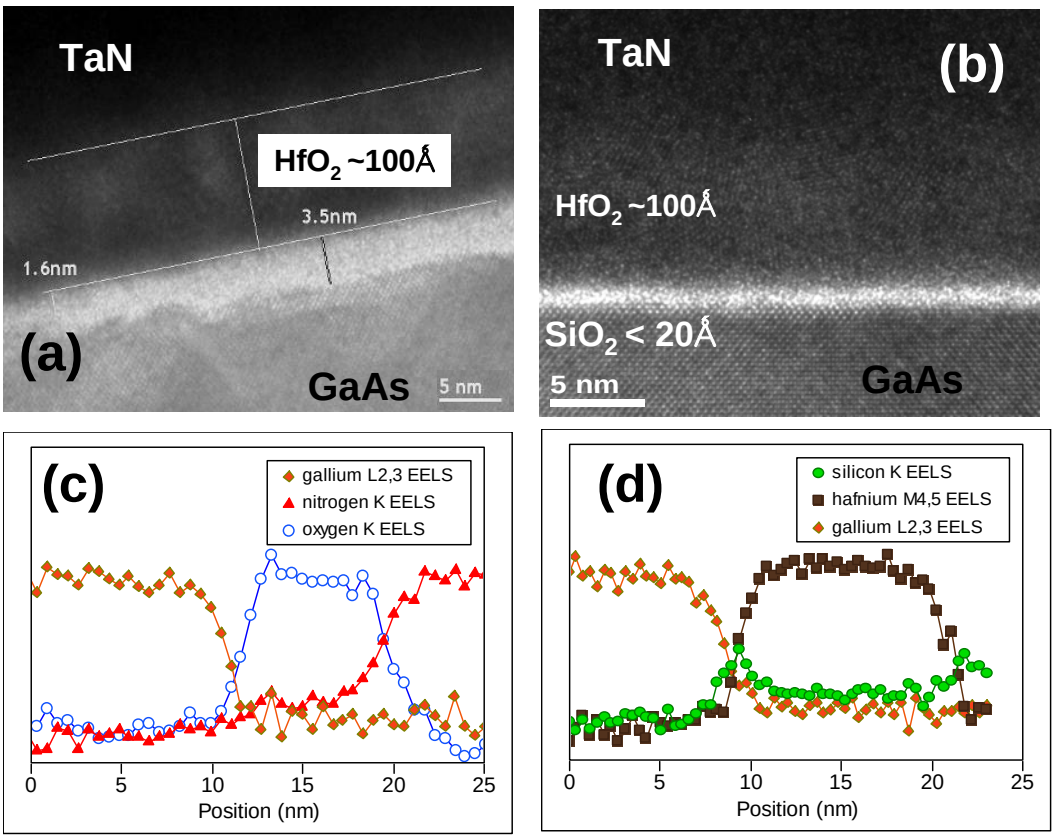

Figure 2.15. (a) Sample W/O Si IPL and PDA of 600°C 3min in $N_2(O_2$ 5%) (b), (c) and (d) Sample with 1 min Si IPL as deposited with EELS analysis

Fig. 2.16(b) TEM with EELS (Fig. 2.16c) and energy dispersive X-ray spectroscopy (EDXS) (Fig. 2.16d) show that Si with 1 min IPL was fully oxidized while protecting GaAs surface and Ga_2O_3 and As_2O_3 increasing on surface resulted in C-V degradation. IPL thickness also changed. X-ray photoelectron spectroscopy (XPS) also show similar result in that with 1 min Si deposition time, Si was partially oxidized, and after 1min PDA in $N_2(O_2$ 5%), the Si IPL was oxidized to SiO_2 (Fig. 2.17a). However, if 2min and

3min Si IPL thickness was used, Si was not fully oxidized even after 15min PDA at 600°C (Fig. 2.17b and Fig 2.17c).

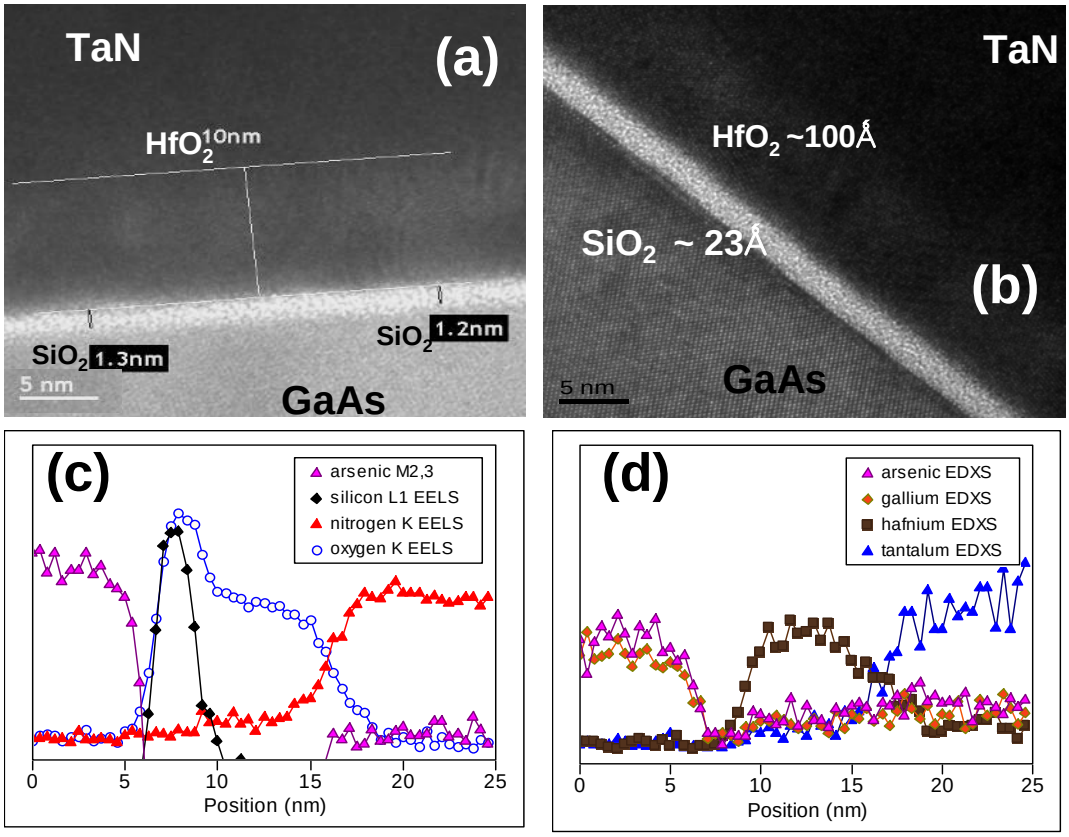

Figure 2.16. (a) A cross-sectional high resolution transmission electron microscopy (HRTEM) image for sample 1min Si IPL and PDA of 600°C 10min in $N_2(O_2$ 5%) (b), (c) and (d) Sample 1 min Si IPL and PDA of 700°C 5min in $N_2(O_2$ 5%) with EELS and EDXS analysis

Flat band voltage shift with different metal gate also provided good evidence for unpinned Fermi level (Fig. 2.18). Metal gate was fabricated by using lift-off process. Using Si passivation layer (1min), flatband voltage shifts according to metal electrode on n-type GaAs which suggests good interface quality and unpinned Fermi level. Si deposition time of 60 second with 7min PDA time resulted in lower D_{it} value using conductance method (Fig. 2.19).

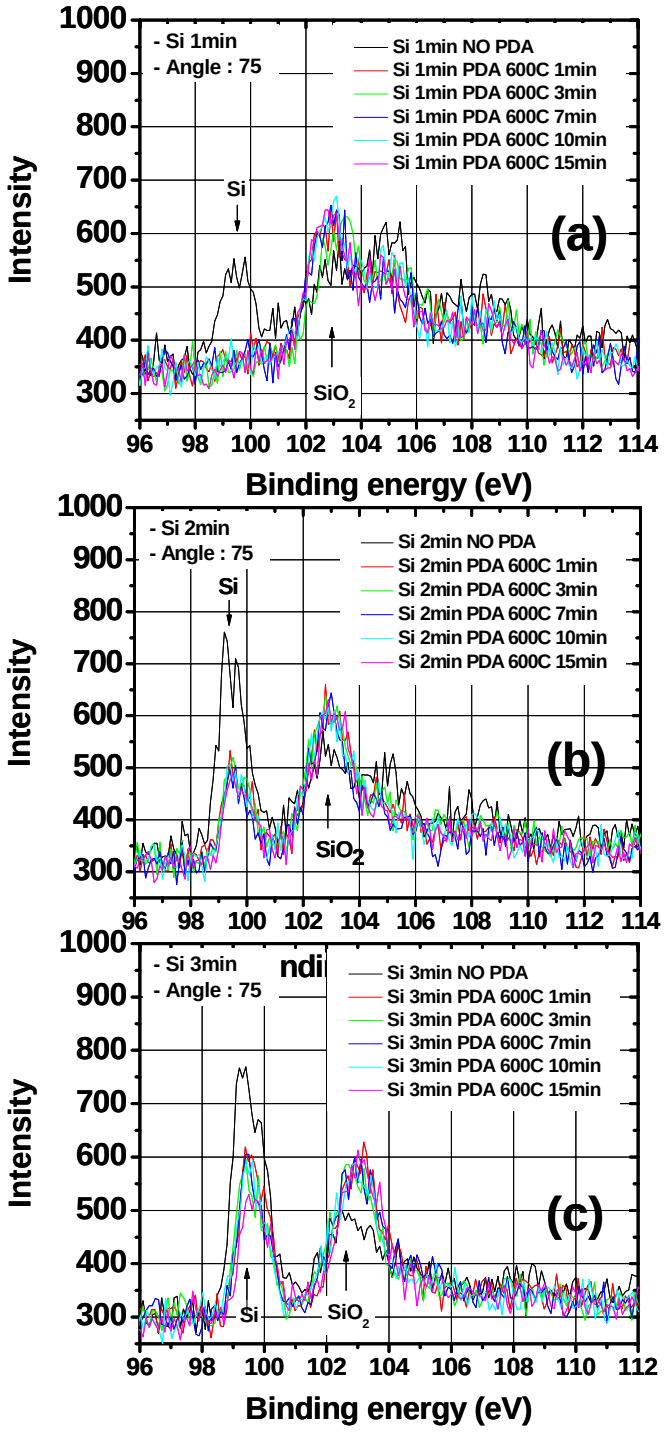

Figure 2.17. XPS for 1, 2, and 3min Si IPL as a function of PDA time

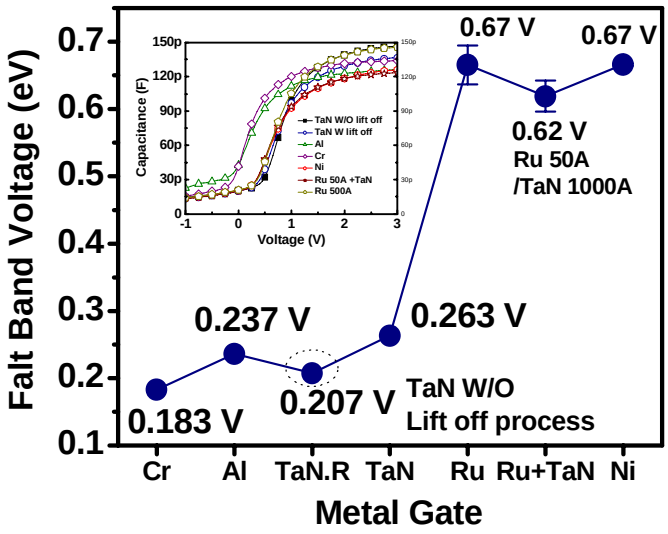

Figure 2.18. Flat band voltage shift with different metal gates on n-type GaAs substrate.

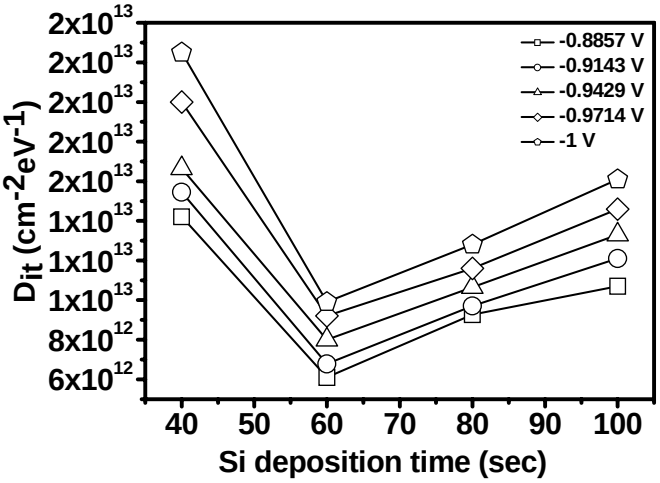

Figure 2.19. D_{it} versus Si IPL deposition condition with PDA 7 min

D_{it} measured by conductance method with parameter adjustment for 7min PDA. Fig. 2.20(a) demonstrates the linear dependence of the equivalent oxide thickness (EOT) on

the physical thickness of HfO_2 with PVD Si 1min passivation with PDA 7min. The k-value of the gate HfO_2 was found to be k=19.5 (with k SiO_2 = 3.9) [31]. Leakage current was reduced (to ~10^{-5} A/cm2) by using the Si IPL for 4.0nm thick high-k dielectric in N-type GaAs wafer (Fig. 2.20b).

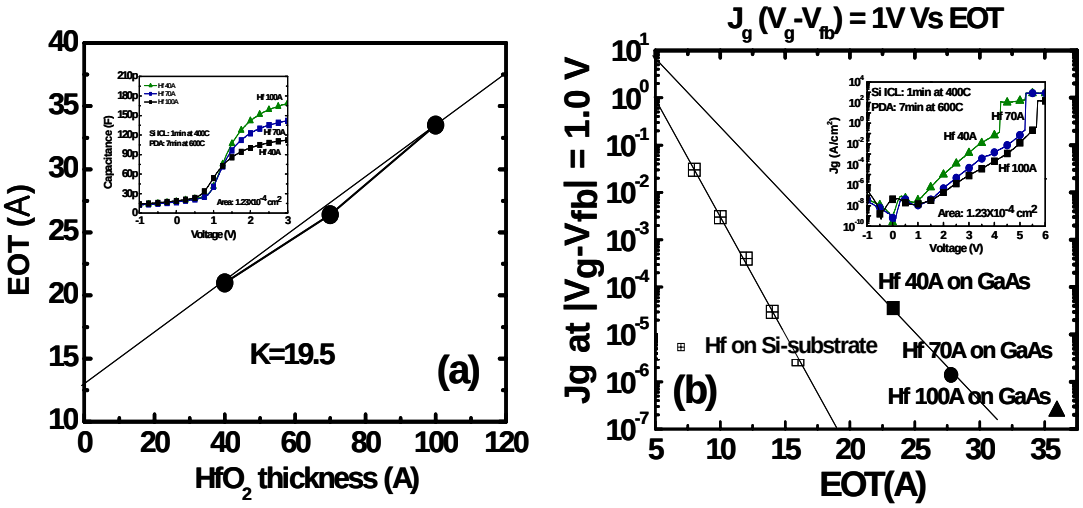

Figure 2.20. (a) EOT versus physical thickness for HfO_2 (b) J_g versus EOT of HfO_2 with PVD Si passivation

2.3.2 Demonstration of depletion mode transistor

We have demonstrated depletion mode MOSFET using the optimum thickness and PDA condition (1 min Si deposition time (≈ 0.8-1nm) and 7min PDA) of the Si passivation layer. The schematic cross section and top view (ring-type) of depletion mode GaAs MOSFET with Si passivation is shown in Fig. 2.21. The thickness of molecular beam epitaxy (MBE) grown n-type GaAs epi-layer layer on semi-insulating substrate was 40nm with Si dopant concentration in the epi-layer of 3×10^{17} cm^{-3}.

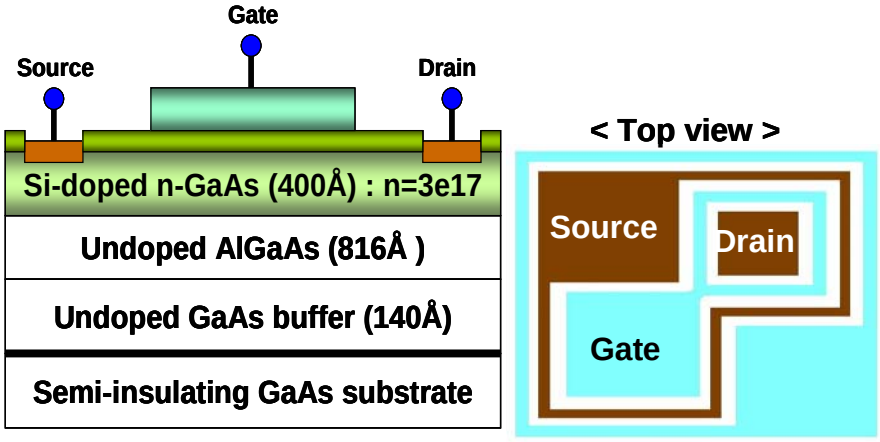

Figure 2.21. Schematic cross section and top view of depletion mode GaAs MOSFET with Si Passivation

The I_d-V_g characteristics are shown in Fig. 2.22(a).

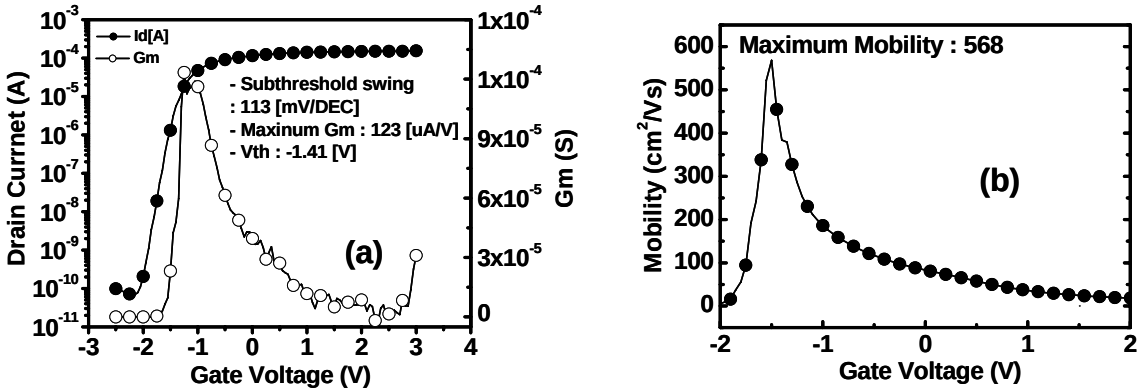

Figure 2.22. (a) Id-Vg and Gm of depletion mode GaAs MOSFET (b) Mobility of depletion mode GaAs MOSFET with Si passivation (W 400μm× L 5μm)

Depletion mode MOSFET with PVD Si passivation layer shows V_T of -1.41V, excellent off-current I_{off} of 69pA, transconductance Gmmax of 123μA/V and swing S of 113mV/dec with width 400μm and length 5μm at drain voltage (V_d) =50mV. Electron mobility for GaAs MOSFET with PVD Si passivation was estimated to be 568cm^2/Vs.

Fig. 2.22(b). Fig. 2.23 show the Id-Vd characteristics that I_{d_max} =2.58 mA at V_g-V_{th} = 1 V.

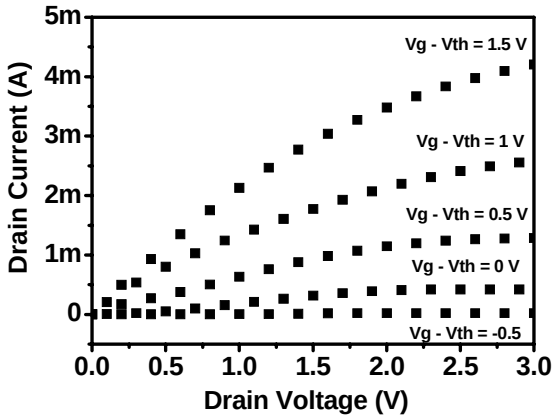

Figure 2.23. Id-Vd of depletion mode GaAs MOSFET with PVD Si passivation (W 400µm× L 5µm)

Output characteristics of MOSFET with I_{dmax} of 2.58 mA at Vg-Vth = 1 V and high series resistance was observed

2.4 DEMONSTRATION OF ENHANCEMENT MODE TRANSISTOR

2.4.1 MOSCAP characteristics on GaAs Substrate with PMA

In this work, using Si IPL we present the electrical characteristics of TaN/HfO_2/GaAs both p- and n-MOSFET made on GaAs substrates with excellent electrical and reliability characteristics, thin EOT (~2.3-3.0nm), low frequency dispersion (< 5%) and high maximum mobility (1213 cm^2/V-s) with high temperature PMA for n-MOSFET on undoped GaAs. Good inversion behavior with low D_{it} on lightly doped p-type GaAs has

been obtained. P-channel GaAs high-k MOSFETs with excellent peak mobility have also been demonstrated.

The Si IPL on undoped GaAs exhibited a small roughness of 0.086nm (see Fig. 2.24 for atomic force microscopy result).

Figure 2.24. Sruface roughness (RMS: 0.086 nm) after Si IPL deposition at 400 °C

After hafnium deposition at room temperature and PDA, Si was fully oxidized (Fig. 2.25) for 3 and 7 min PDA samples of undoped GaAs. Note that for longer Si deposition time (>80 sec), Si was not fully oxidized even after 10min PDA (Fig. 2.25). Photoluminescence (PL) was measured with different Si deposition time as function of PDA. Peak signal of PL increased when Si was changed to SiO_2 especially for Si 1min IPL (Fig. 2.26). After PMA at 900°C, frequency dispersion of 60-80sec IPL devices were still in excellent range (~ 5%, $\Delta V<100$ mV) (Fig. 2.27). D_{it} measured by conductance method was improved for thicker (80sec Si deposition time) IPL samples (Fig. 2.28) compare to 60sec Si deposition time.

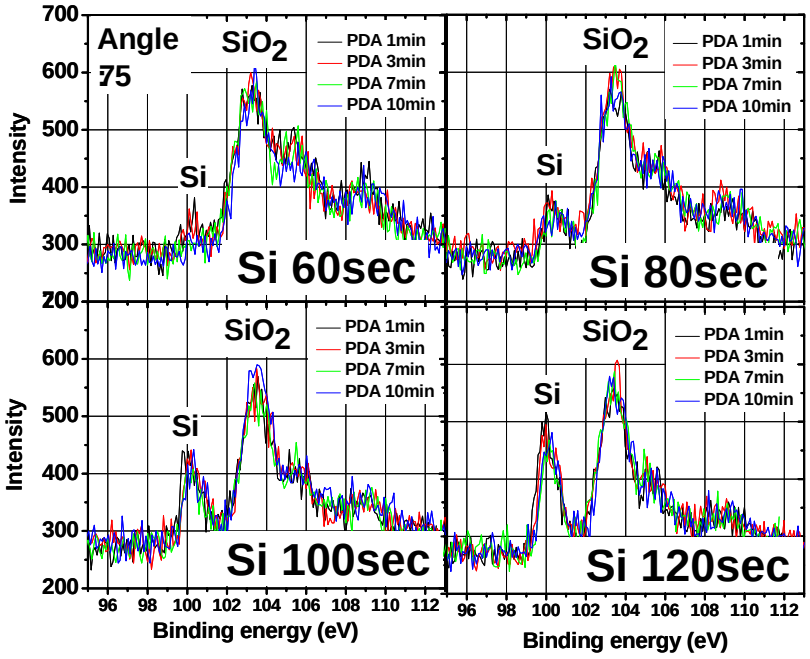

Figure 2.25. XPS with 1~10 min PDA with 60~120 sec Si deposition time on undoped GaAs wafer

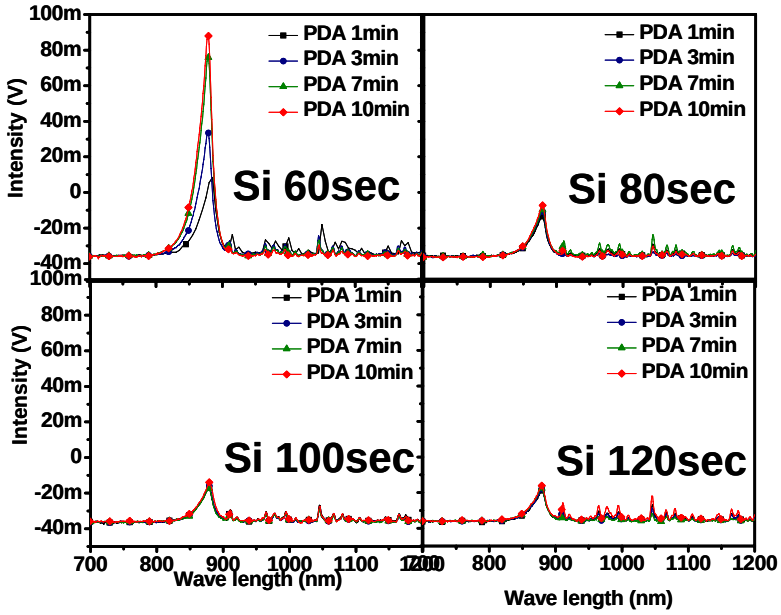

Figure 2.26. PL with 1~10min PDA with 60~120sec Si deposition time on undoped GaAs wafer

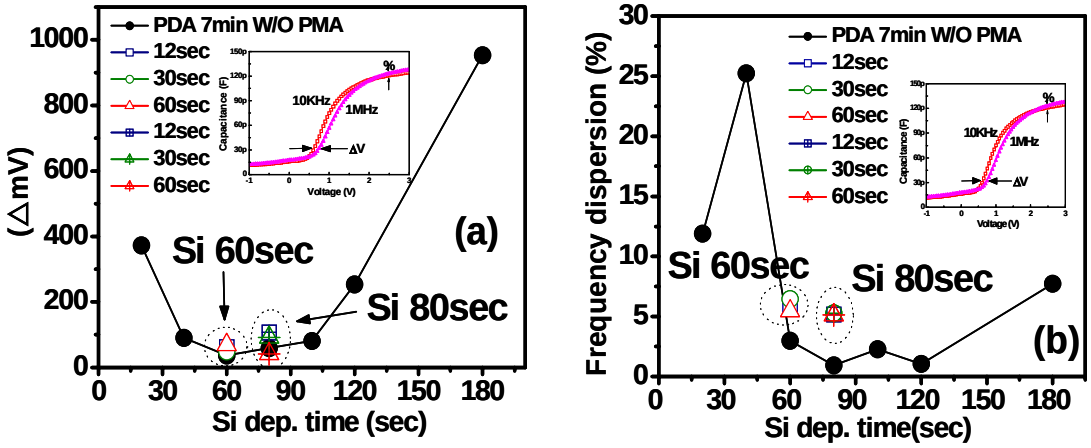

Figure 2.27. Frequency dispersion (ΔmV and %) with PMA 900°C 12~60sec and Si 60 and 80sec thickness

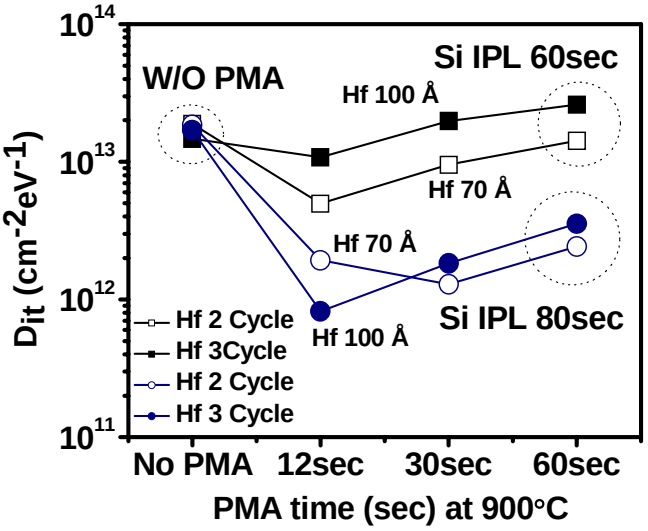

Figure 2.28. D_{it} with PMA 900°C 12~60sec with Si 60sec and 80sec deposition time using conductance method

In Fig. 2.29, the leakage current values as function of EOT are compared. The leakage currents of PMA samples were also found to improve with slightly thicker IPL. Using Si

passivation (60sec deposition time and 7min PDA), flat band voltage shifted according to different metal electrodes on p-type GaAs (Fig. 2.30), which suggests good interface quality and unpinned Fermi level.

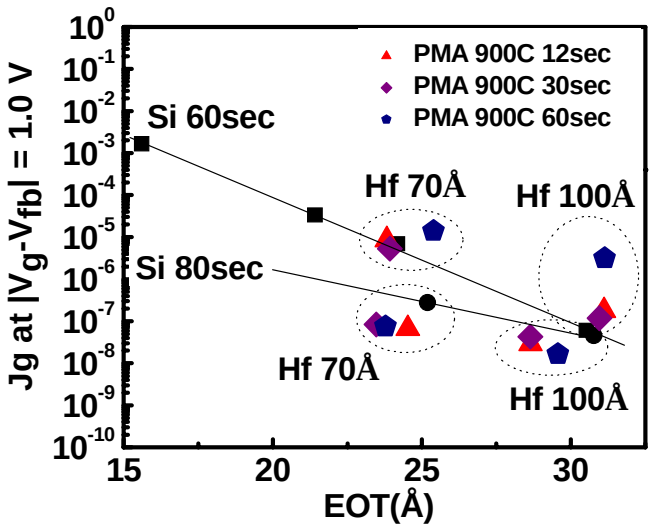

Figure 2.29. Jg versus EOT of HfO_2 70Å and 100Å with PVD Si passivation 60sec and 80sec thickness after PMA

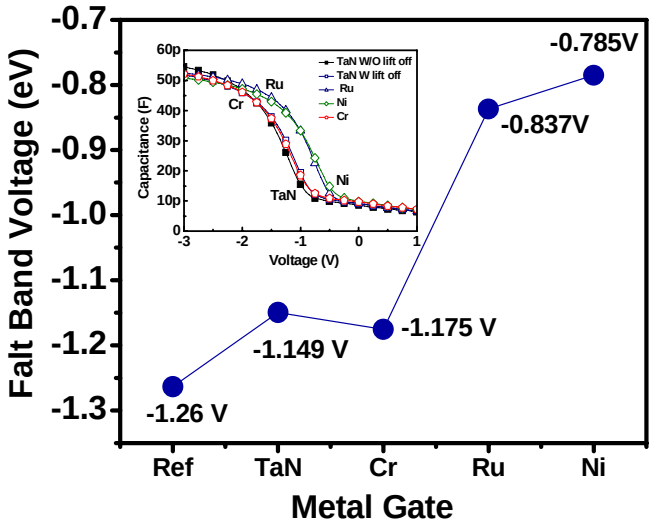

Figure 2.30. Flat band voltage shift with different metal gates on p-type GaAs substrate

2.4.2 MOSFET characteristics on undoped GaAs Substrate

N-MOSFETs on undoped GaAs substrate using the Si IPL (80sec) and 750°C PMA were fabricated. The schematic cross section and top view of n-MOSFET with Si passivation is shown in Fig. 2.31.

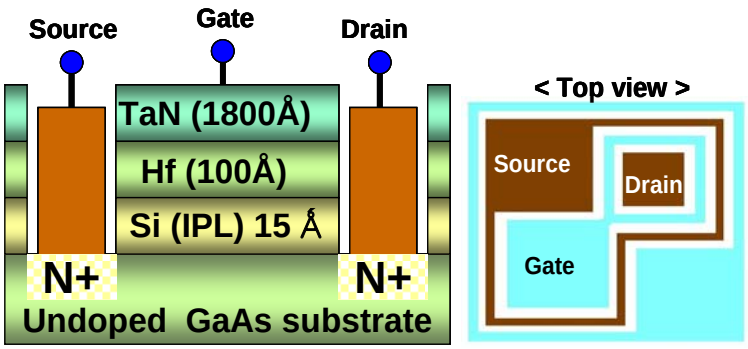

Figure 2.31. Schematic cross section and top view of NMOSFET with Si passivation 80sec

Inversion C-V curves for frequency from 1 kHz to 1MHz were very close each other (Fig. 2.32).

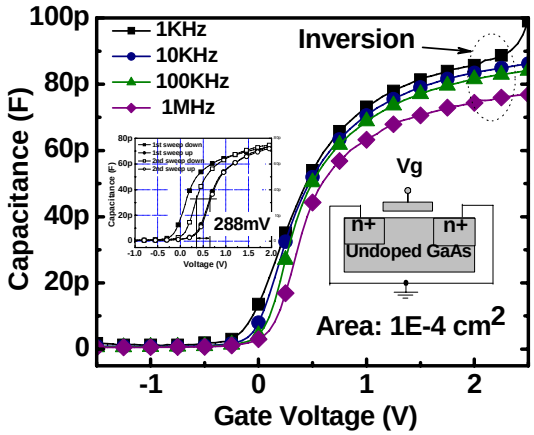

Figure 2.32. Frequency dispersion in inversion area of NMOSFET with Si 80sec and PMA 750°C

Using inversion capacitance (Fig. 2.33a) and Id-Vg (Fig. 2.33b), high peak mobility (1213 cm^2/V-s) has been obtained for n-MOSFET on undoped GaAs. N-channel MOSFET with PVD Si passivation layer shows V_{th} of 0.24V, excellent on-off ratio of ~10^7, transconductance G_{m_max} of 516.7μA/V and swing S of 121.81mV/decade with width 800μm and length 10μm at drain voltage (Vd=50mV); along with excellent Id-Vd characteristics that $Id_{\_max}$ =12.2 mA at V_g-V_{th} = 2.0 V. (Fig. 2.34).

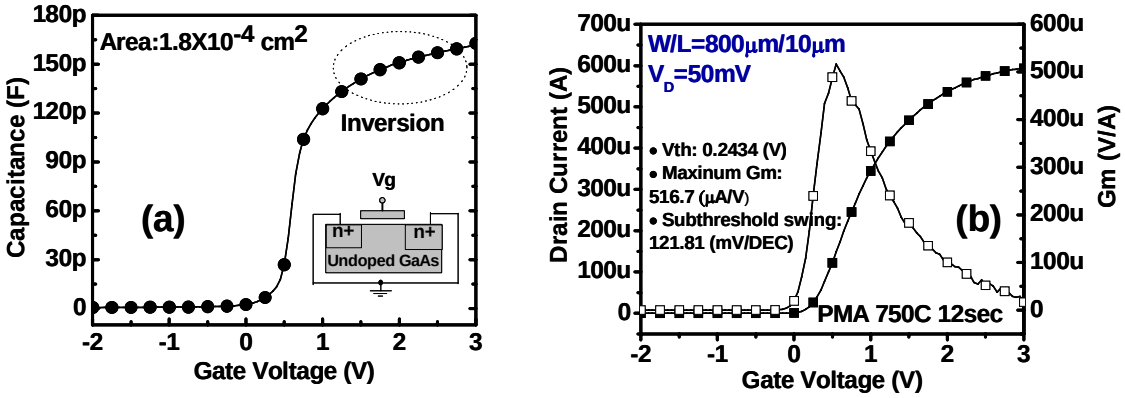

Figure 2.33. (a) Inversion C-V characteristic between gate and source combined with drain (b) Id-Vg and Gm of n-MOSFET with Si passivation (W800μm× L 10μm) with peak Gm 516.7 (μA/V)

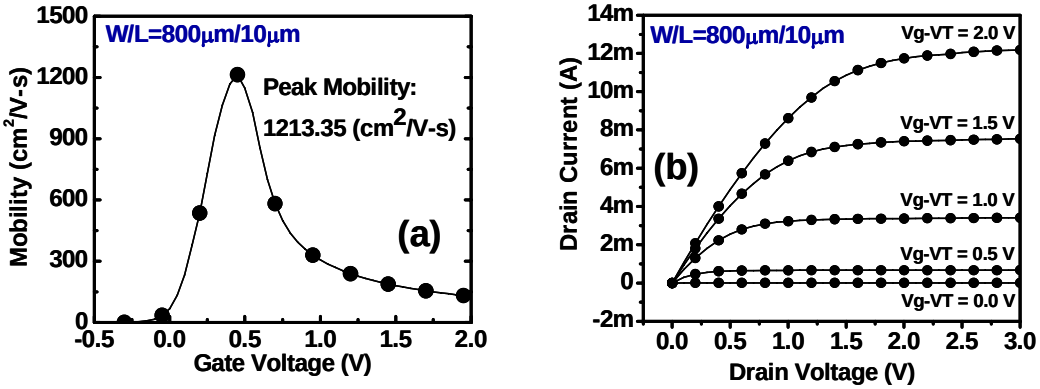

Figure 2.34. (a) Mobility (b) I_d-V_d of NMOSFET with Si passivation (W800μm× L 10μm)

Identical layout for p-MOSFET with varying PMA temperature 750°C-900°C on undoped GaAs was used with schematic cross section shown in Fig. 2.35.

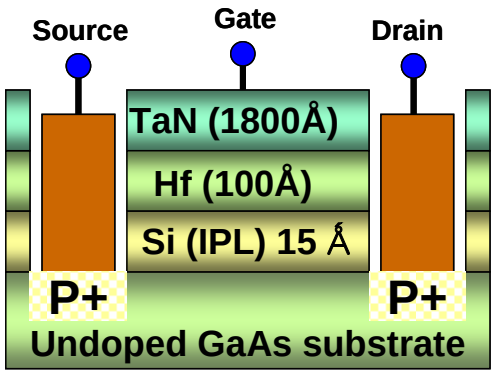

Figure 2.35. Schematic cross section of p-MOSFET on undoped GaAs substrate with Si passivation 80sec

Frequency dispersion with inversion capacitance between 1MHz and 100KHz was found to be large for p-MOSFET (Fig. 2.36a).

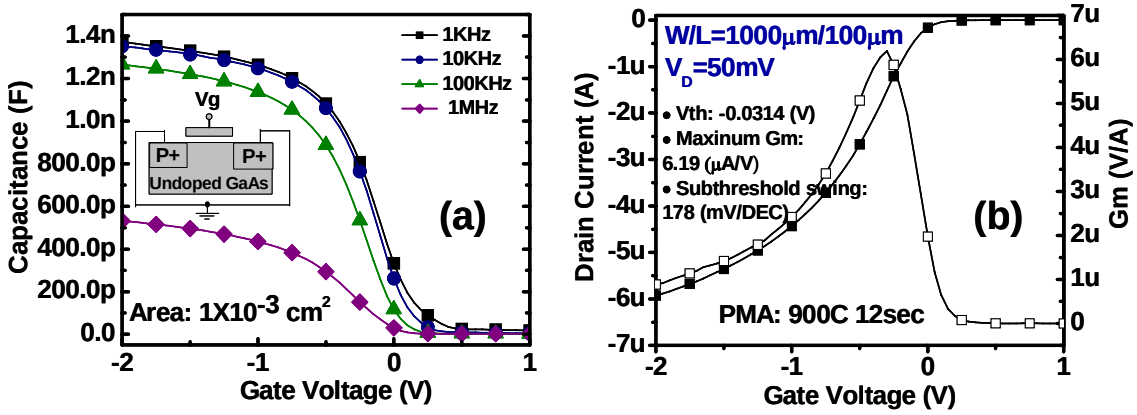

Figure 2.36. (a) Frequency dispersion in inversion area of p-MOSFET with Si passivation 80sec (b) Id-Vg and Gm of p-MOSFET with Si passivation (W1000µm× L 100µm)

Using the inversion capacitance and Id-Vg (Fig. 2.36b), excellent peak mobility (191 cm^2/V-s) has been obtained for p-MOSFET on undoped GaAs substrate, along with well-

behaved Id-Vd characteristics (Fig. 2.37). With increasing PMA temperature, 1MHz inversion capacitance increased along with improved frequency dispersion, higher peak G_m and mobility (Fig. 2.38).

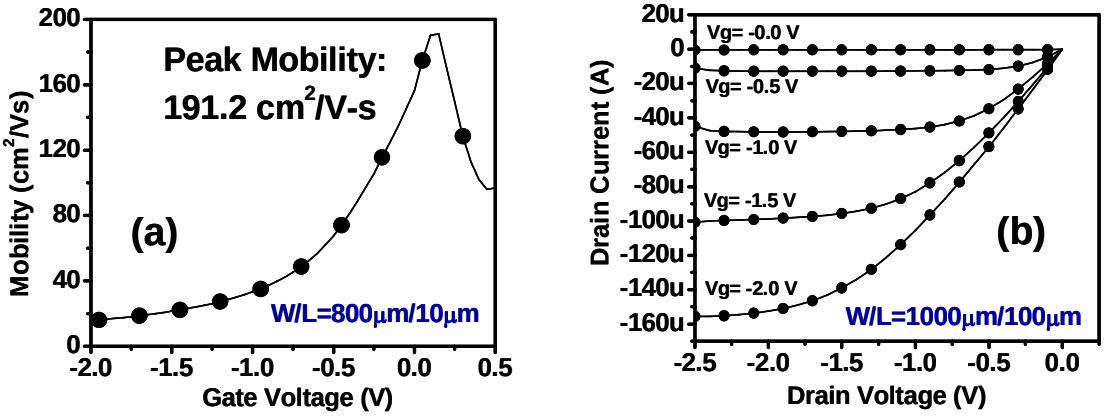

Figure 2.37. (a) Mobility (b) I_d-V_d of p-MOSFET with Si passivation (W1000μm× L 100μm)

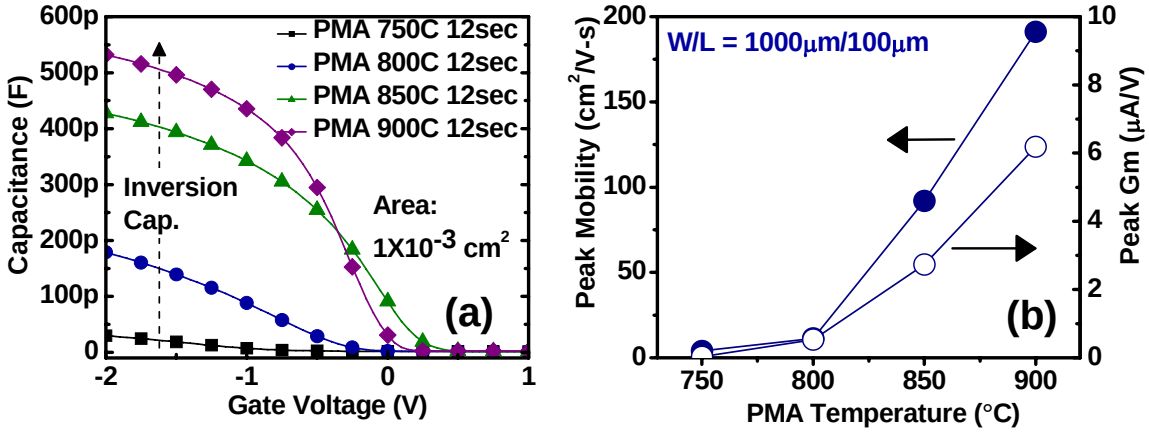

Figure 2.38. (a) Inversion capacitance improvement (b) Mobility and Peak G_m improvement with different PMA 750°C 12sec - 900°C 12sec

2.4.3 n-MOSFET characteristics on p-GaAs Substrate

Using lightly doped p-type ($1\times10^{16}cm^{-3}$) grown in molecular beam epitaxy (MBE) on p-type GaAs, n-MOSFETs with Si IPL of 80sec and 750°C PMA were fabricated. The schematic cross section of p-MOSFET with Si passivation is shown in Fig. 2.39.

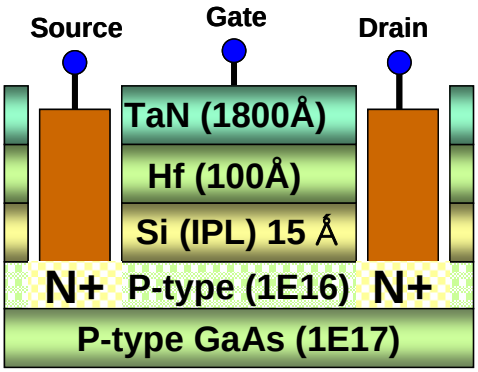

Figure 2.39. Schematic cross section of NMOSFET with Si passivation 80sec on lightly doped P-type GaAs substrate

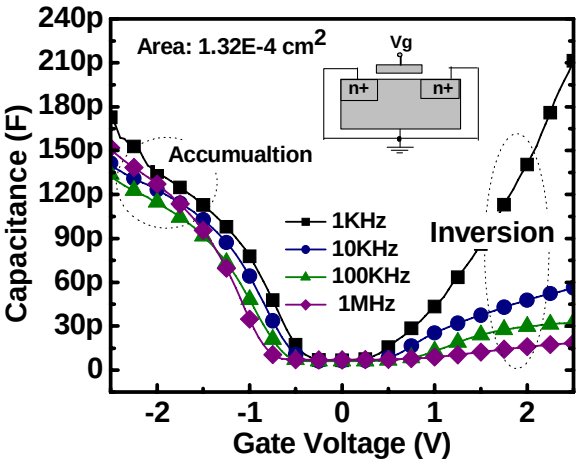

Figure 2.40. Frequency dispersion in accumulation and inversion area of NMOSFET with Si 80sec thickness

Accumulation C-V frequency dispersion was reasonable, however, inversion C-V curves for frequency between 1MHz and 1KHz had large difference because source and drain

region were not fully activated (Fig. 2.40). Id-Vg and Id-Vd characteristics are shown in Fig. 2.41.

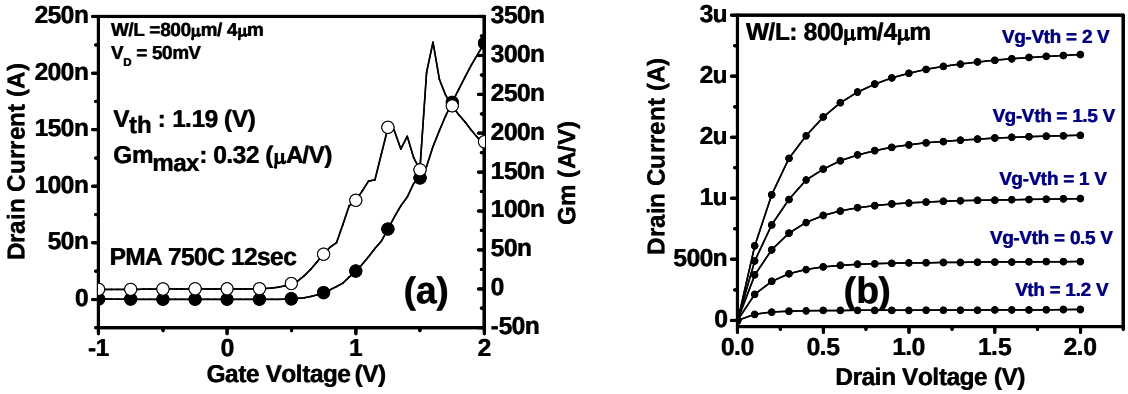

Figure 2.41. (a) Id-Vg and G_m (b) I_d-V_d of n-MOSFET with Si passivation (W800μm× L4μm) with lightly doped P type GaAs substrate

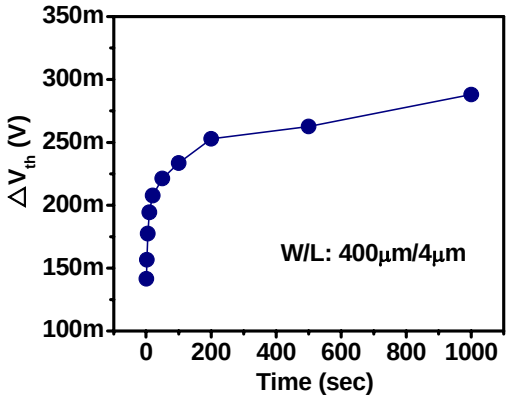

Figure 2.42. Stress induced V_{th} shift of NMOSFET with Si passivation (W400μm× L4μm) on lightly doped P type GaAs substrate with 750°C PMA

Electrical stress has been applied to examine reliability characteristics of these high-k GaAs MOSFETs (e.g. stress-induced V_{th} shift in Fig. 2.42). The threshold voltage shift magnitude was similar to stress induced V_{fb} on MOSCAP on n-type GaAs (Fig. 2.43).

Voltage shift was more depended on Hf thickness than on Si IPL thickness. Using charge pumping technique, D_{it} value of ~1.2×10^{12} (Fig. 2.44) was obtained, which is similar to what was obtained from conductance method (Fig. 2.28).

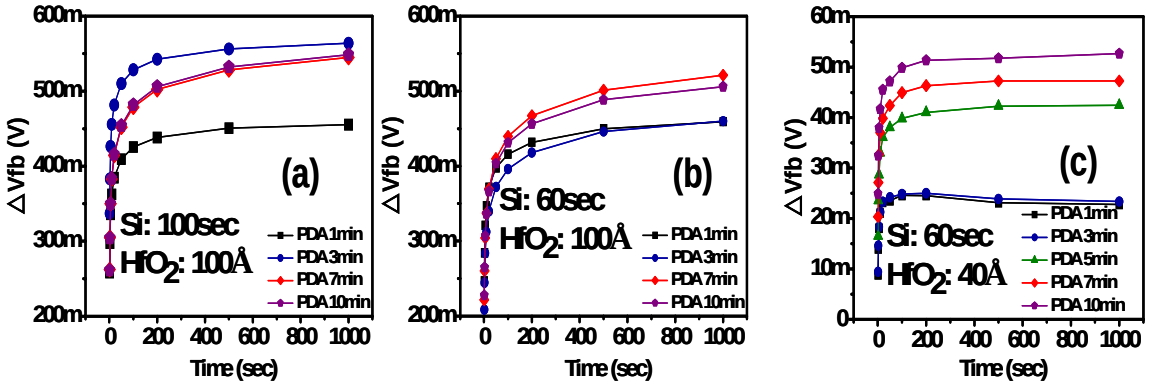

Figure 2.43. Stress induced Vfb shift of MOSCAP with Si 60 and 100sec passivation and Hf 100Å and 40 Å on n type GaAs wafer without PMA

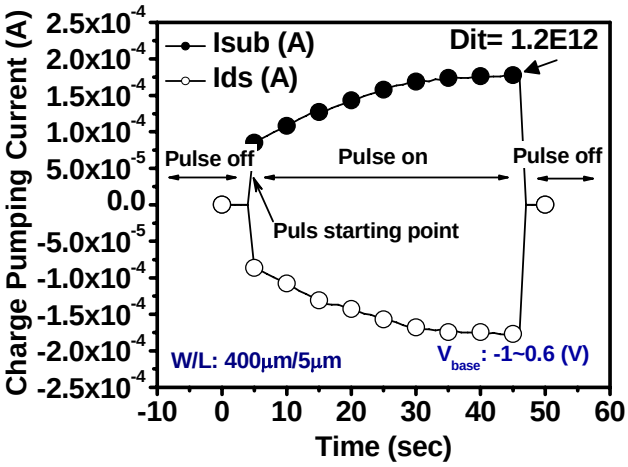

Figure 2.44. Charge pumping currents measurement for evaluation of the interface density (D_{it}) with NMOSFET (W400µm× L5µm) with lightly doped P-type GaAs substrate

2.5 TEMPERATURE EFFECTS OF SI INTERFACE PASSIVATION LAYER DEPOSITION ON GAAS MOS CHARACTERISTICS

In this work, we studied the electrical characteristics of TaN/HfO_2/GaAs MOS capacitors with Si IPL under various PDA (post-deposition anneal) condition and various Si deposition temperature/time. Using optimal Si IPL under reasonable PDA, PMA conditions and various Si deposition temperature, excellent electrical characteristics with low frequency dispersion (<5%, and 50mV) and reasonable D_{it} value (~10^{12} $eV^{-1}cm^{-2}$) can be obtained. It was found that higher temperature of Si IPL deposition and longer PDA time at 600°C improved EOT and leakage current.

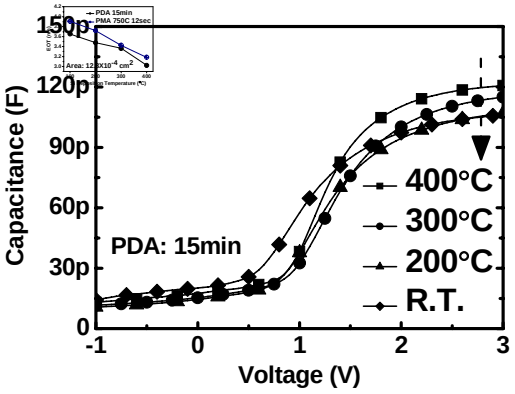

Figure 2.45. 1MHz CV characteristics of MOSCAPs with 1.2 nm thick of amorphous Si IPL as function of Si IPL deposition temperature. (EOT versus Si deposition temperature in inset figure)

Fig. 2.45 shows C-V characteristics on the MOSCAP with 10nm thickness of HfO_2 with Si 80sec deposition time (1.2nm) and PDA 600°C 15min condition varying

temperature. The inset of Fig. 2.45 depicts EOT versus Si IPL deposition temperature with increasing deposition temperature, accumulation capacitance increased (i.e. EOT decreased), possibly due to densification of Si IPL layer at higher temperature. It has also been reported that the Si IPL with lower deposition temperature could be easier to be oxidized, which would result in thicker EOT .

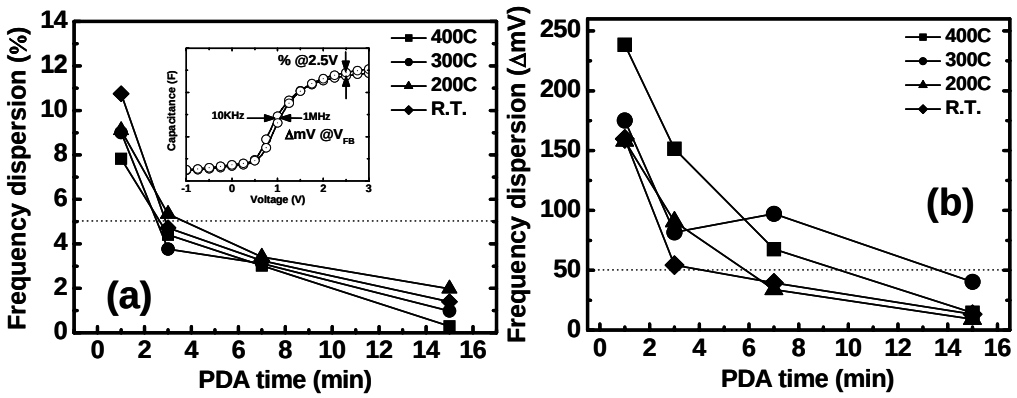

Figure 2.46. Frequency dispersion versus PDA time as a function of Si IPL deposition temperature: (a) capacitance difference (%) between 1MHz and 10KHz and (b) voltage difference (mV) at flat band voltage

Fig. 2.46(a) and 2.46(b) summarizes the frequency dispersion characteristics versus PDA time as a function of Si deposition temperature. The definition of frequency dispersion, % $((C_{10KHz}-C_{1MHz})/C_{1MHz}\times 100$ [%] at 2.5V) and ΔmV (voltage differences between 1 MHz and 10 KHz of C-V at flat band voltage) is shown in inset of Fig. 2.46a. With longer PDA time, low frequency dispersion (< 5% and <50mV) can be obtained. This is due to more complete oxidation of the Si IPL layer and consequently reduced charge trapping. It has been found that the thinner the remaining unoxidized Si IPL layer is, the higher interface quality. This can be explained by the quantum control well model

or simply reduced charge trapping due to the reduced thickness of the highly trapped unoxidized Si layer. PDA time has more impact on frequency dispersion than Si IPL deposition temperature. High PMA temperature reduced frequency dispersion to < 5% even for those samples with short time PDA (e.g. 1min) which had larger frequency dispersion compare to longer time PDA samples before PMA in Fig. 47(a, b). This is due to additional oxidation during PMA.

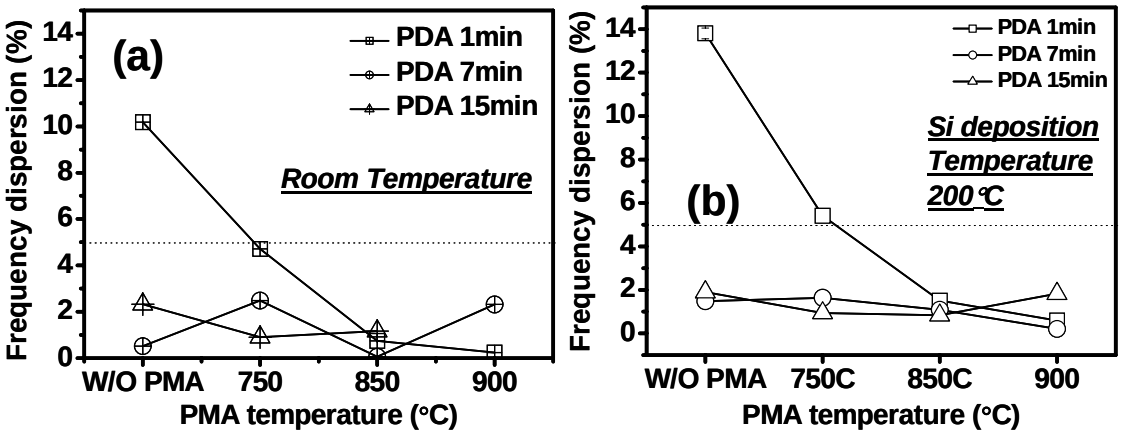

Figure 2.47. Frequency dispersion versus PDA time as a function of Si IPL deposition temperature: (a) frequency dispersion versus PMA time with different PDA time of Si deposition condition at room temperature (b) Si deposition condition at 200 ºC

In general, longer PDA time lead to lower hysteresis and D_{it} value for n-MOSCAP (Fig. 2.48). D_{it} follows the similar trend as frequency dispersion (Fig. 2.48a). The results support the contention that a fully oxidized Si IPL would provide a lower D_{it} and thus a better interface quality. In general, longer PDA time led to lower hysteresis, possibly due to the reduction of charge trapping in the high-k layer (Fig. 2.48b). Fig. 2.49 shows the leakage current density at V_g-V_{FB}=1 versus equivalent oxide thickness (EOT)

with different Si deposition temperature. In general, higher Si deposition temperature led to lower Jg, possibly due to densified Si IPL which prevents As out-diffusion.

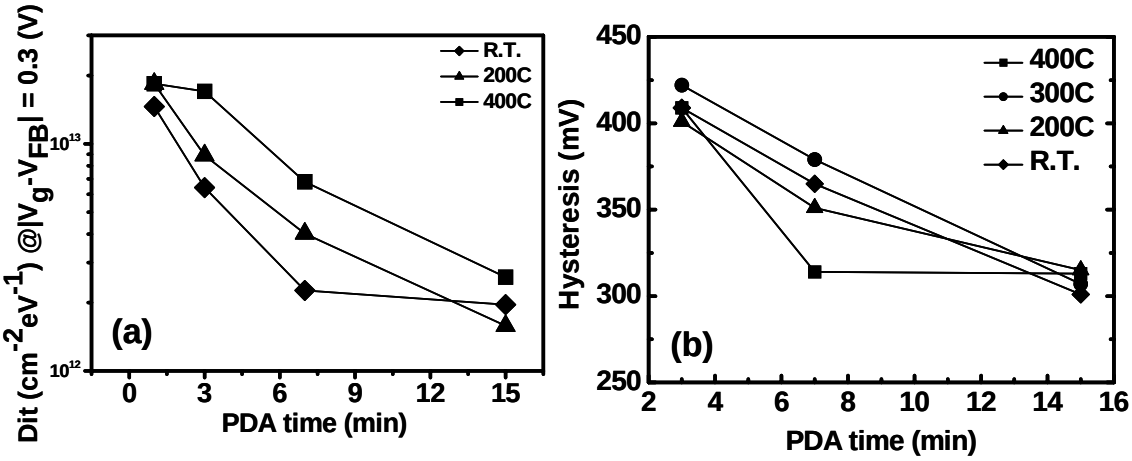

Figure 2.48. (a) D_{it} by using conductance method with parameter fitting at V_{fb}-0.3V (b) Hysteresis for 1MHz CVs (sweep rate: 500mV/sec) versus PDA time as function of Si deposition temperature.

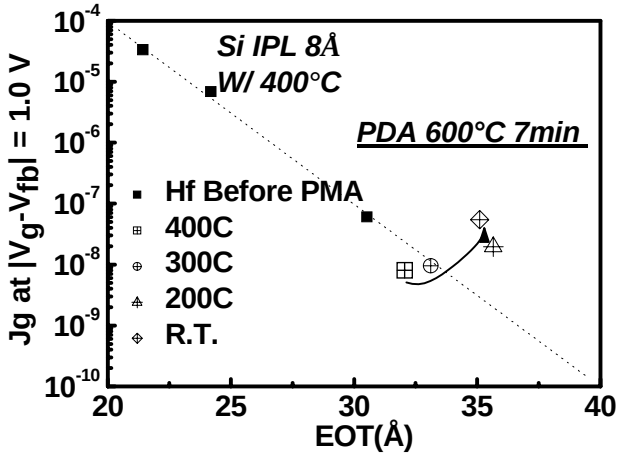

Figure 2.49. Leakage current density versus EOT as a function of Si IPL deposition temperature.

2.6 POST-METAL-ANNEALING OPTIMIZATION OF SELF-ALIGNED N- CHANNEL GAAS MOSFETS USING HfO_2 AND SILICON IPL

This work presents the electrical characteristics of TaN/HfO_2/GaAs self-aligned n-MOSFET with Si IPL under various PMA conditions and different substrate doping concentrations. MOS capacitors were fabricated on p-type GaAs (100) doped with Zn and undoped GaAs (100) wafer. After Si and Zn ion implantation for source and drain (S/D) of nMOSFET and pMOSFET, respectively, a RTA of 750°C-950°C for 12sec-60sec was used for S/D activation.

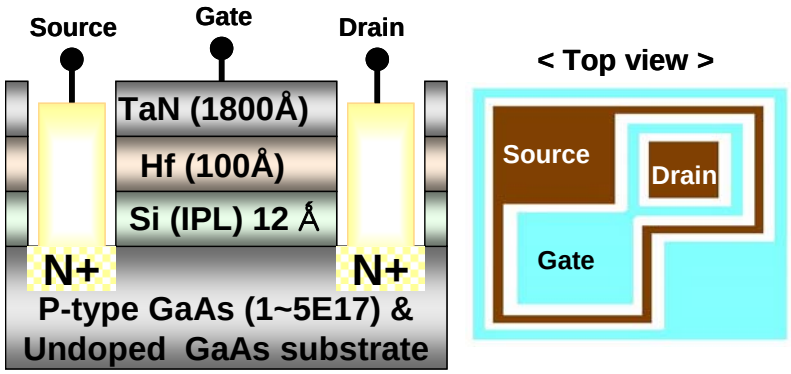

Figure 2.50. Top view and Schematic cross section of n-MOSFET with Si 1.2nm

Using the optimized process, TaN/HfO_2/GaAs n-MOSFETs made on p-GaAs substrates exhibit good electrical characteristics. The schematic cross section and top view of n-MOSFET with Si passivation is shown in Fig. 2.50. The minimum thickness of the Si IPL layer preventing Fermi level pinning at GaAs-HfO_2 interface was found to be ~1.2 nm (PVD deposition time 80sec) for transistor fabrication with high temperature PMA [32-33]. Fig. 2.51 (a) shows I_d and $G_{m,\,max}$ versus different PMA condition. For S/D activation, Zn was more easily activated than Si (pMOSFET) and Si was more easily

activated in undoped GaAs than p-type GaAs (nMOSFET). Using 80sec Si IPL, Excellent C-V characteristics in both accumulation and inversion region after PMA 950ºC 1min were observed in Fig. 2.51 (b).

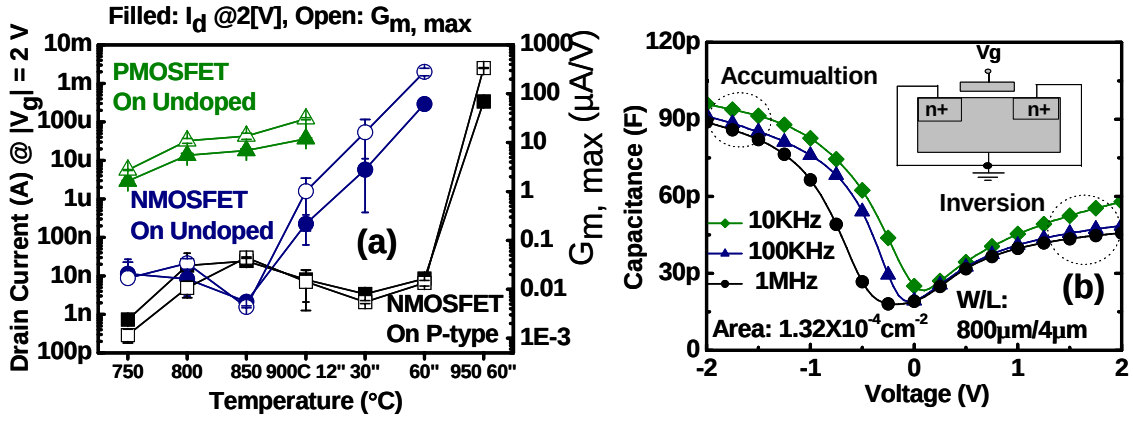

Figure 2.51 (a) I_d at $|V_{gate}|$ = 2[V] (filled symbol) and $G_{m, max}$ (filled symbol) versus PMA temperature and time (750°C 12sec, 800°C 12sec, 850°C 12sec, 900°C 12sec, 900°C 30sec, 900°C 60sec, and 950°C 60sec, respectively) with 1.2nm Si IPL (80 sec deposition time) for p-MOSFET and n-MOSFET (b) Accumulation and Inversion C-V of n-MOSFET with 1.2 nm Si IPL on p-type (PMA 950°C 1min) GaAs (n-MOSFET)

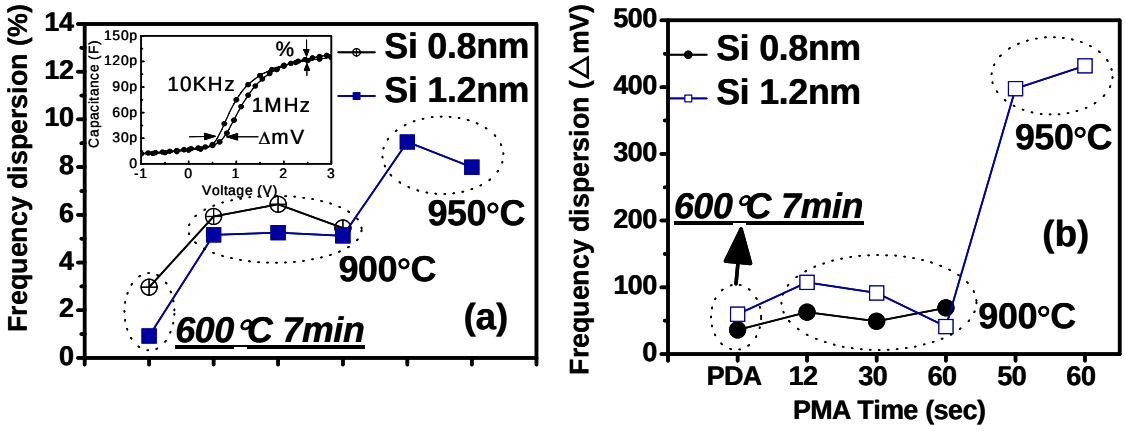

Figure 2.52 Frequency dispersion of (a) capacitance difference (%) between 1MHz and 10KHz and (b) voltage difference (mV) at flat band voltage of n-MOSFET with 0.8nm (60sec Si deposition time) 1.2 nm (80sec Si deposition time) Si IPL after 950°C PMA (PDA only and 900°C PMA condition were shown for comparison)

After PMA 950°C 1min, frequency dispersion (Fig. 2.52 (a) and (b)) was degraded compare to less than 900°C 1min PMA condition. Frequency dispersion % and ΔmV are definition of $(C_{10KHz}-C_{1MHz})/C_{1MHz}\times100$ [%] at 2.5V and V_{1MHz} - V_{10KHz} at V_{FB} of V_{1MHz} defined in Fig. 2.52 a). In general, longer Si deposition time and higher PMA temperature led to lower hysteresis (Fig. 2.53 (a)).

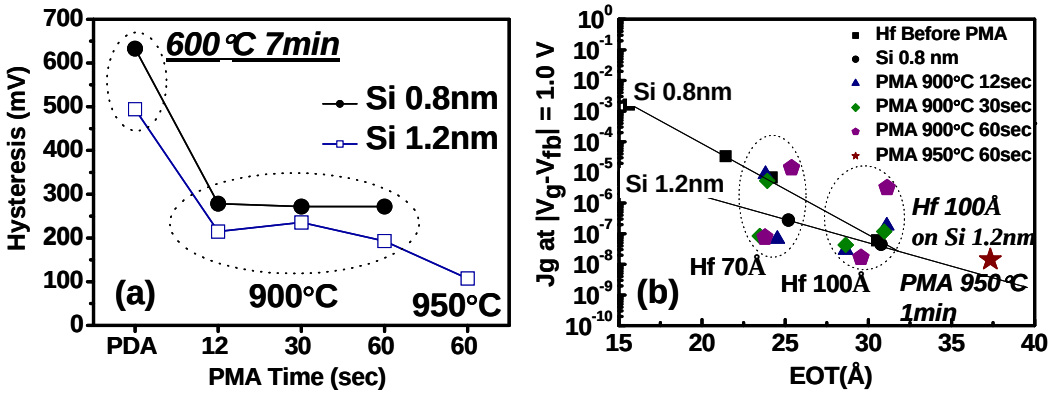

Figure 2.53 (a) Hysteresis for 1MHz CVs (sweep rate: 500mV/sec) (b) leakage current density versus EOT of n-MOSFET with 1.2 nm Si IPL after 950°C PMA (PDA and 900°C PMA condition were shown for comparison)

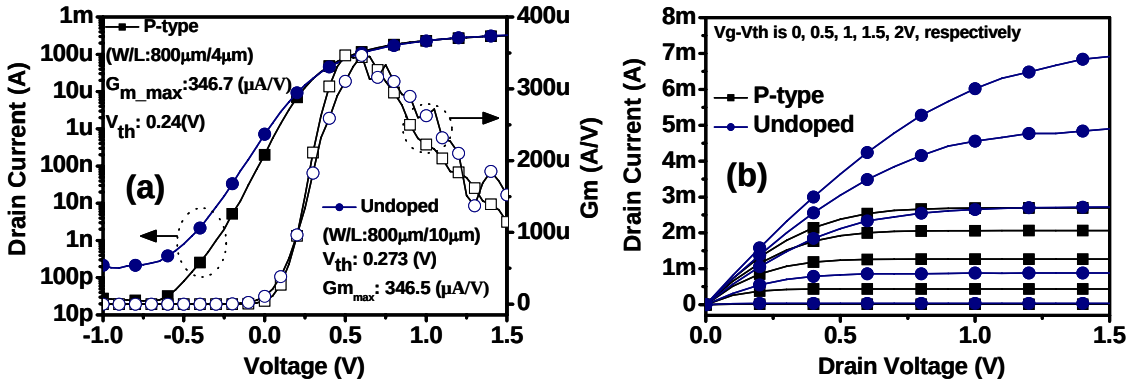

Figure 2.54 (a) I_d-V_g (b) I_d-V_d of n-MOSFET on undoped GaAs with PMA of 900°C 60sec and on p-type with PMA of 950°C 60sec

Leakage current remains low (Fig. 2.53 (b)). Drain current along with $G_{m,max}$ and mobility for n-MOSFET on undoped GaAs and low PMA (900°C 60sec) thermal budget shows better characteristics than n-MOSFET on p-type GaAs with PMA of 950°C 1min (Fig. 2.54 (a), (b), and 2.55(a)).

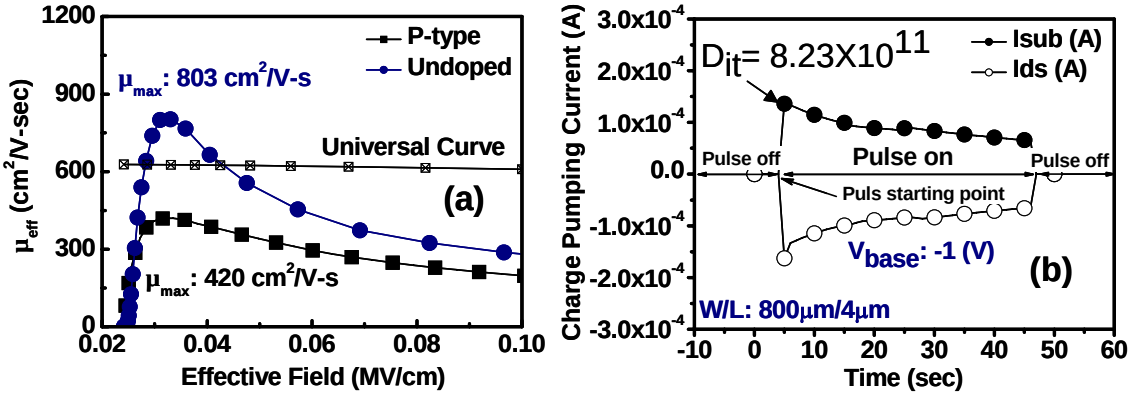

Figure 2.55 (a) mobility of n-MOSFET on undoped GaAs with PMA of 900°C 60sec and on p-type with PMA of 950°C 60sec and (d) Charge pumping of n-MOSFET on p-type with PMA of 950°C 60sec

Using inversion capacitance and I_d-V_g, peak mobility has been obtained for n-MOSFETs. In general, lower substrate doping concentration is required for n-MOSFET fabrication. From the charge pumping technique, D_{it} of 8.23×10^{11}/ (cm^2·eV) was obtained for n-MOSFET on p-type GaAs subatrate with PMA 950ºC 1min in Fig. 2.55 (b).

2.7 INFLUENCE OF THE SUBSTRATE ORIENTATION ON THE ELECTRICAL AND MATERIAL PROPERTIES OF GAAS METAL-OXIDE-SEMICONDUCTOR (MOS) CAPACITORS AND SELF-ALIGNED TRANSISTORS USING HFO_2 AND SILICON INTERFACE PASSIVATION LAYER (IPL)

The optimum thickness of the Si layer preventing Fermi level pinning at GaAs-HfO_2 interface was found to be ~1.2 nm (Si deposition time 80 sec) for MOSFET

fabrication. In this paper, we studied the influence of the substrate orientation on the electrical and material characteristics of TaN/HfO_2/GaAs GaAs n-type Metal-Oxide-Semiconductor Capacitors (NMOSCAP) and PMOSCAP and self-aligned n-MOSFETs. There have been only a few reports on the orientation dependence of GaAs substrates [34-37]. In this work, electrical characteristics with frequency dispersion, D_{it} and peak mobility with high temperature PMA for three different orientations on GaAs of n-MOSFET have been compared. The results suggested that orientation dependence can be explained by using GaAs/Si coupling energy [35-36].

MOS capacitors were fabricated on n-type and p-type ($1\sim5\times10^{17}/cm^3$) GaAs wafer doped with Si and Zn for different orientation (100), (110), and (311). A cross-sectional view of the MOSCAP structure is shown in Fig. 2.56.

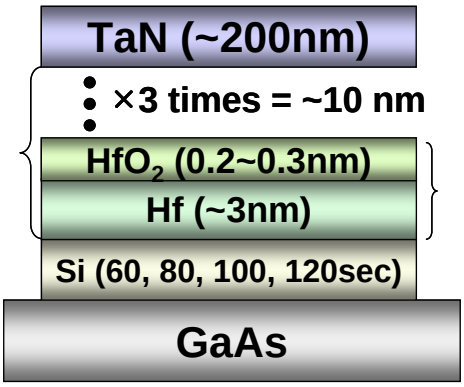

Figure 2.56. A cross-sectional view of the MOSCAP structure for MOS capacitors on GaAs ($1\sim5\times10^{17}/cm^3$) wafers.

Fig. 2.57(a) and 2.57(b) summarize the frequency dispersion characteristics (% definition of $(C_{1KHz}-C_{1MHz})/C_{1MHz}\times100$ [%] at 2.5 V) and ΔmV (definition of $|V_{1MHz}-V_{1KHz}|$ at V_{fb} defined in inset of Fig. 2.57(a)) versus different deposition time with 7 min PDA at 600ºC and different PDA time with 60 sec Si deposition time (Fig 2.58a and

2.58b). With PDA of 7min, 60sec was minimum thickness to unpin the Fermi level (Fig 2.57a and 2.57b).

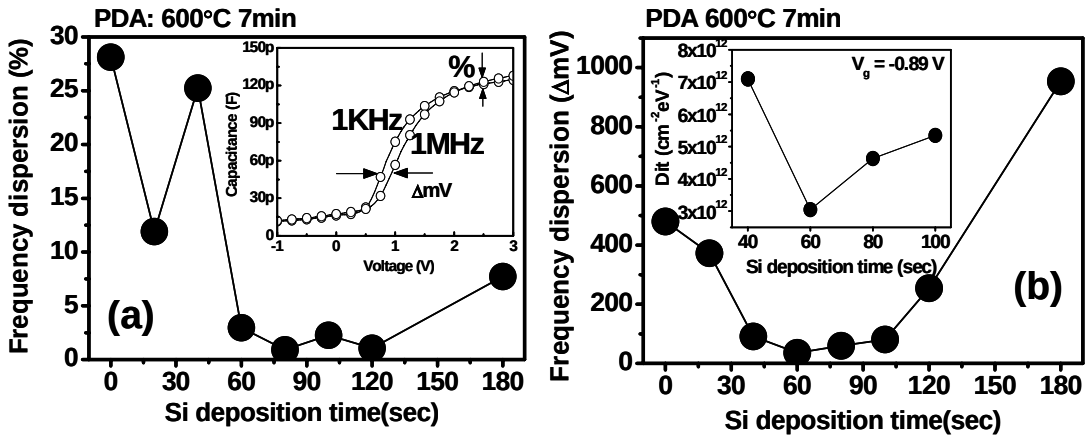

Figure 2.57. (a) Frequency dispersion of %, definition of $(C_{1KHz}-C_{1MHz})/C_{1MHz}\times100$ [%] at 2.5V (b) Frequency dispersion of ΔmV, definition of $|V_{1MHz}-V_{1KHz}|$ at V_{fb} defined in inset of Fig. 2.57a, versus different Si deposition time with 7 min PDA at 600ºC (D_{it} comparison with Si IPL of 40sec, 60sec, 80sec, and 100sec with PDA 600 ºC 7min)

However samples with thicker than Si 60sec deposition time show worse frequency dispersion and D_{it} compare to Si 60sec deposition (inset of Fig. 2.57b). D_{it} was measured by using conductance method with parameter fitting at V_{fb}-0.89V for each p-type GaAs samples. Among the different PDA time and temperature but with a fixed thickness of Si (60 sec deposition times), PDA time of 7 min shows the smallest frequency dispersion. This implies the lowest interface trap densities. With increasing PDA time at 600ºC, Si was continuously oxidized to SiO_2 (XPS results in inset of Fig. 2.58a) and this oxidation improved the frequency dispersion up to 7min PDA. Beyond 7 min of PDA, the frequency dispersion started to degrade. It is believed to be due to the increasing As_2O_3 and Ga_2O_3 contents (XPS results in inset of Fig. 2.58b).

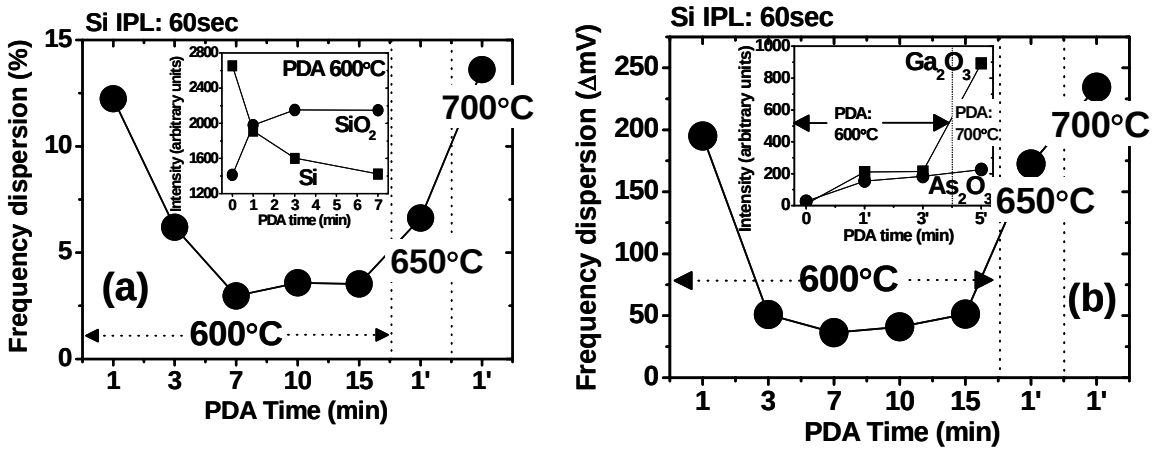

Figure 2.58 (a) Frequency dispersion % (b) ΔmV with different PDA time and 60 sec Si deposition time. Inset of 2.58(a) and 2.58(b) are XPS spectra from reference to peak value for Si, SiO_2, Ga, Ga_2O_3 and As and As_2O_3.

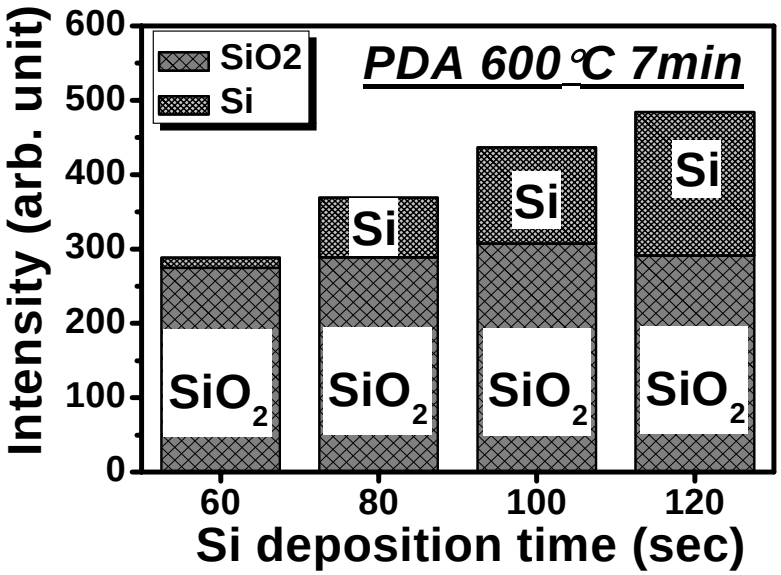

Figure 2.59 Si spectra from reference (minimum line of each XPS intensity) to peak value of Si spectra on GaAs with Si deposition time of 60, 80, 100, 120 sec and PDA of 600ºC 7min

Note that the Ga_2O_3 signal increased significantly if PDA temperature is above 650 ºC with the corresponding severe degradation of frequency dispersion; while the As_2O_3 signal increased just slightly (XPS results in inset of Fig. 2.58b). It can be concluded that Ga_2O_3 might play an important role in affecting interface quality. X-ray photoelectron spectroscopy (XPS) showed that with increasing Si deposition time, the remained Si measured from reference (minimum line of each XPS intensity) to peak value of Si spectra on GaAs increased while the formation of SiO_2 saturated at a range. Small amount of Si with 60sec Si deposition time shows that almost all Si IPL transformed to SiO_2 (Fig 2.59). The interfacial quality is affected by PDA condition and can be improved by formation of less Ga_2O_3, As_2O_3 and unoxidized Si. Fig. 2.60 shows XPS results for different substrate on (100), (110), and (311) with and without PDA. As shown in Fig. 2.60 (a) and 2.60 (b), As_2O_3 and SiO_2 were obtained due to the PDA anneal. The formation of SiO_2 and As_2O_3 was similar after PDA of 600 ºC 7 min (Fig. 2.60 a-b). In particular the (110) shows the highest intensity of Ga_2O_3 spectra and the (100) shows the lowest intensity (Fig 2.60 c). Interface state density measurement (D_{it}) shows that the (100) oriented substrate exhibits slightly better interface quality on both n-type and p-type in Fig 2.60 (d). In terms of frequency dispersion of MOSCAPs, the (100) oriented substrate also exhibits slightly lower % values (Fig. 2.61a). The result suggests that (100) orientation exhibits the lowest interface defect density and PDA can be used to reduce these defects. However, the frequency dispersion (%) of MOSCAPs on each different orientation substrates was found to be very similar with different PDA condition (Fig. 2.61b).

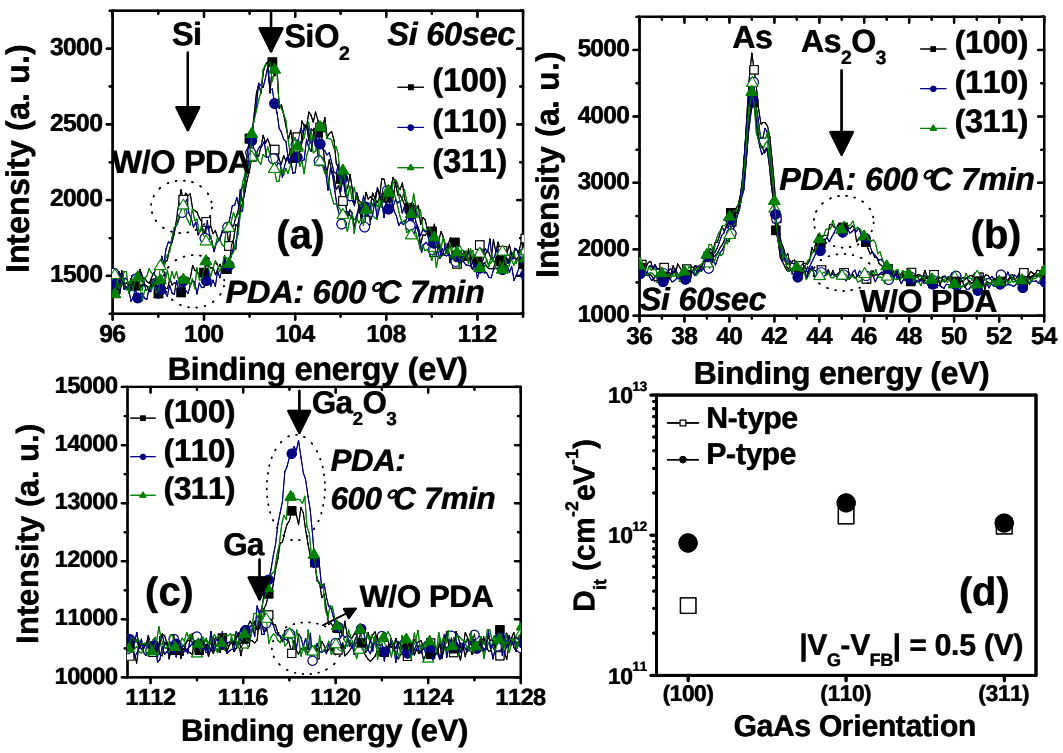

Figure 2.60. XPS spectra of (a) Si and SiO_2 (b) As and As_2O_3 (c) Ga and Ga_2O_3 with (empty) and without (filled) PDA of 600ºC 7 min on GaAs with Si IPL of 60 sec deposition time. (d) D_{it} measured by conductance method at $|V_g - V_{fb}| = 0.5$ (V) using parameter adjustment on n-type and p-type GaAs substrate

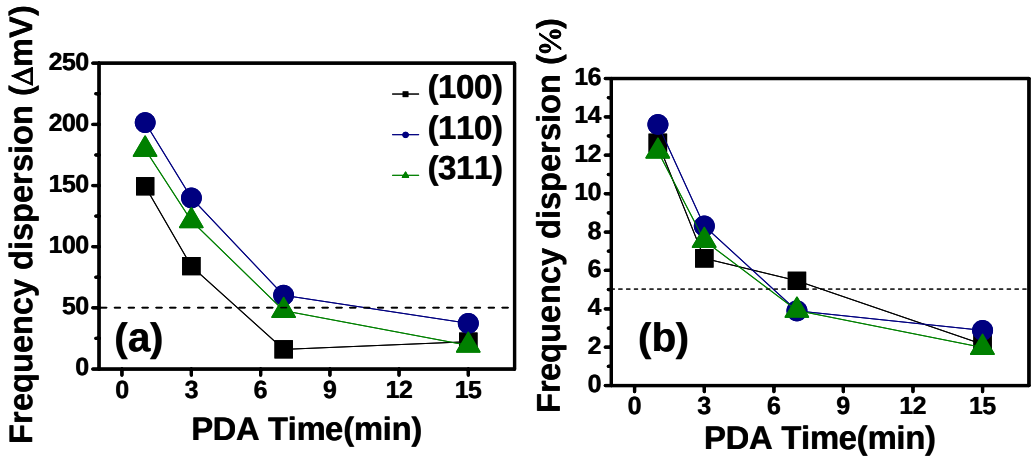

Figure 2.61. (e) Frequency dispersion of ΔmV (f) Frequency dispersion of % with different PDA time at 600ºC and Si 60sec deposition thickness for different orientation

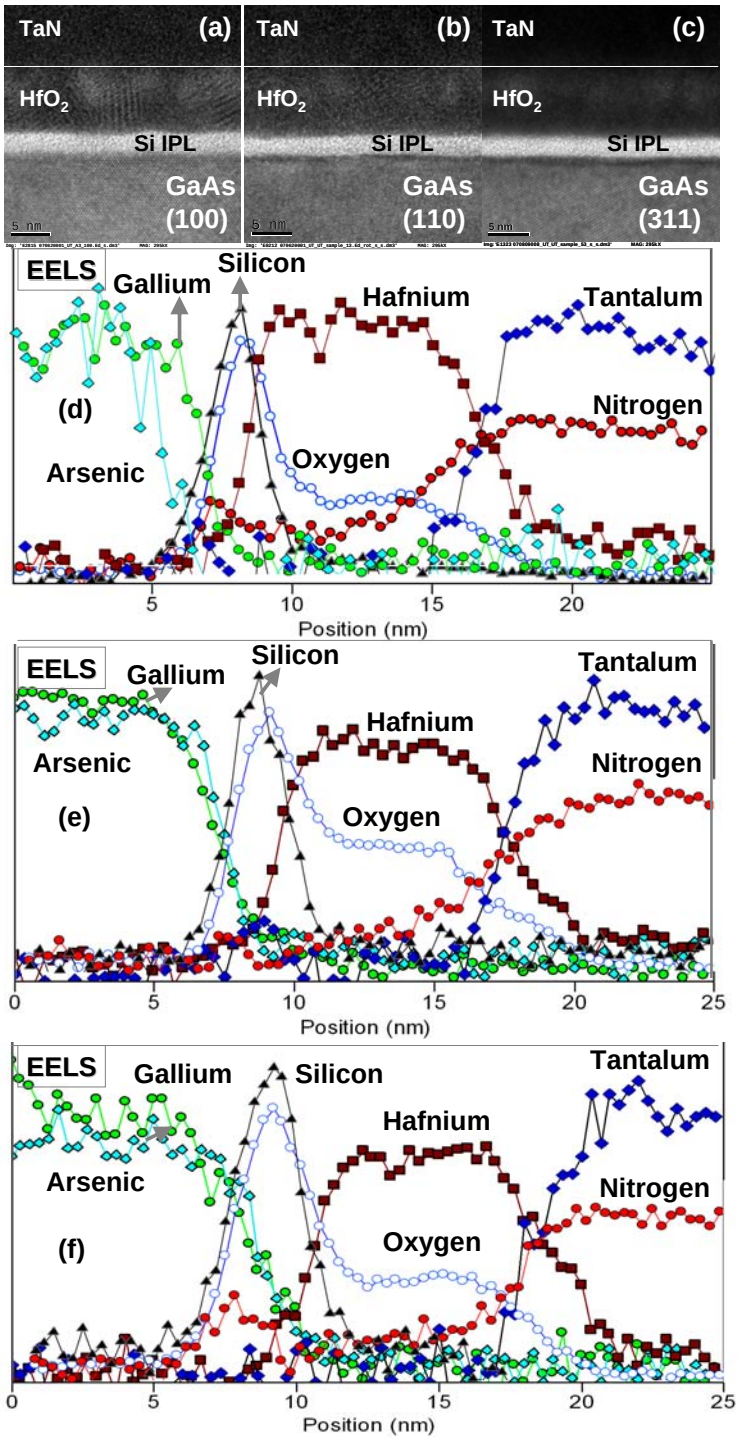

Figure 2.62. A cross-sectional high resolution transmission electron microscopy (HRTEM) image for (a) (100) (b) (110) (c) (311) and energy loss spectroscopy (EELS) for (d) (100) (e) (110) (f) (311) on the nMOSFETs with 10nm HfO_2 and Si 1.5 nm with PDA of 600°C 3 min after PMA of 800°C 30sec

A cross-sectional high resolution transmission electron microscopy (HRTEM) image and energy loss spectroscopy (EELS) on the nMOSFETs with 10nm HfO_2 and Si 1.5 nm with PDA of 600°C 3 min after PMA of 800°C 30sec after gate patterning show similar results for different substrate orientations (Fig. 2.62). EELS show that Si was partially oxidized after PMA process (Fig. 2.62d-2.62f).

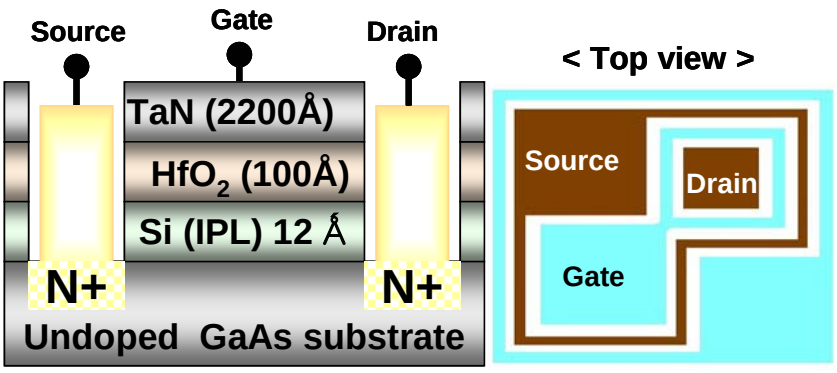

Figure 2.63. The schematic cross section and top view of n-MOSFET with Si Passivation (80 sec deposition time) on undoped GaAs substrate

We fabricated GaAs nMOSFETs employing the same gate stack using a ring-FET geometry consisting of an annular gate on undoped GaAs substrate with different orientation, in order to simplify the device isolation process.). N-MOSFETs using the Si IPL (1.5nm) and 800°C PMA were fabricated using different orientation [(100), (110) and (311)] on undoped GaAs substrates. The schematic cross section and top view of n-MOSFET with Si passivation is shown in Fig. 2.63. Si IPL layer was deposited for transistor fabrication to prevent Fermi level pinning at the GaAs-HfO_2 interface. Orientation of (100) substrate shows better transistor characteristics in terms of drain current versus gate voltage, G_m, drain current versus drain voltage, and mobility (Fig. 2.64a - 2.64d). The effective electron mobility (μ_{eff}) was evaluated for the same device

from the I_d-V_g plot (measured at a drain voltage of 50 mV) and its corresponding split C-V. The improved MOSFET characteristics of (100) devices can be attributed to better interface quality.

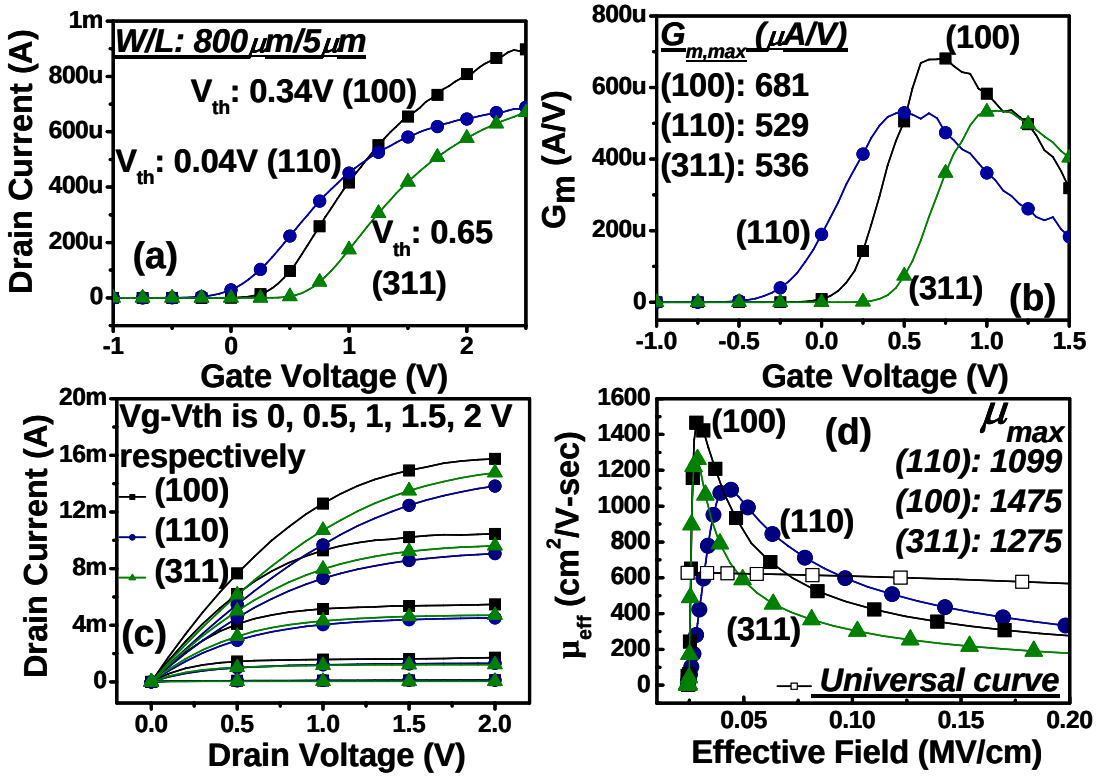

Figure 2.64. (a) Drain current versus gate voltage (b) G_m (c) Drain current versus drain voltage (d) Mobility with different substrate orientation with (100), (110), and (311) for n-MOSFET with Si Passivation (80 sec deposition time) on undoped GaAs substrate

2.8 METAL GATE HfO_2 MOS STRUCTURES ON GAAS SUBSTRATE WITH SIGE INTERFACE PASSIVATION LAYER FOR SCALING DOWN

In this work, we present the electrical characteristics of TaN/HfO_2/GaAs MOS capacitors with SiGe IPL under optimum deposition time and post deposition anneal (PDA) condition. Using different Si and Ge deposition rate, we adjust the Si:Ge ratio in

the SiGe IPL. Thin EOT (~1nm) in Ge-rich IPL, low frequency dispersion (<5%), low hysteresis and low leakage current density in Si-rich IPL have been obtained. MOS structures were fabricated on n-type GaAs wafer doped with Si (1~4) $\times 10^{17}$ cm^{-3}. SiGe IPL was deposited by sputtering of Si and Ge. Fig. 2.65 shows C-V characteristics on the MOSCAP with 7nm thickness of HfO_2 with optimum deposition time and PDA condition at 600°C varying Si:Ge ratio.

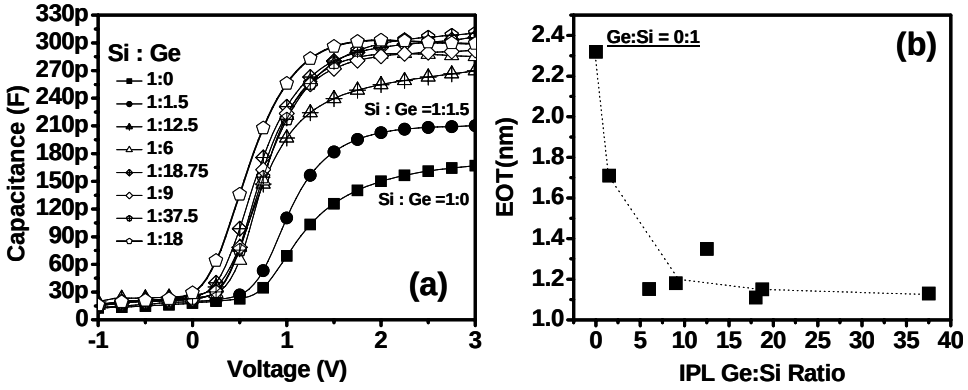

Figure 2.65. (a) C-V with various Si:Ge ratio IPL (b) EOT (nm) versus Ge:Si ratio in IPL

As Ge content increases, V_{FB} shifts in negative direction while inversion capacitance increases. Note that Si deposition rate was 0.8-1 nm/min with 150W and 1.2-1.5 nm/min with 15W, 4.3-4.9 nm/min with 60W and 7.0-8.0 nm/min with 125W for Ge. EOT reduction with increasing Ge content is shown more clearly in Fig. 2.66. For Ge:Si ≥ 18:1, EOT is ~1nm. Frequency dispersion characteristics (% and ΔmV) versus different IPL deposition condition are summarized in Fig. 2.66a and 2.66b. Generally, Ge IPL MOSCAP exhibited larger hysteresis than Si IPL counterpart. Hysteresis also can be adjusted with different Ge:Si ratio (Fig.2.67). Pure Si IPL devices exhibited the least

hysteresis, as expected (Fig. 2.67). Capacitors with Ge-rich IPL have very small process window compare to Si IPL.

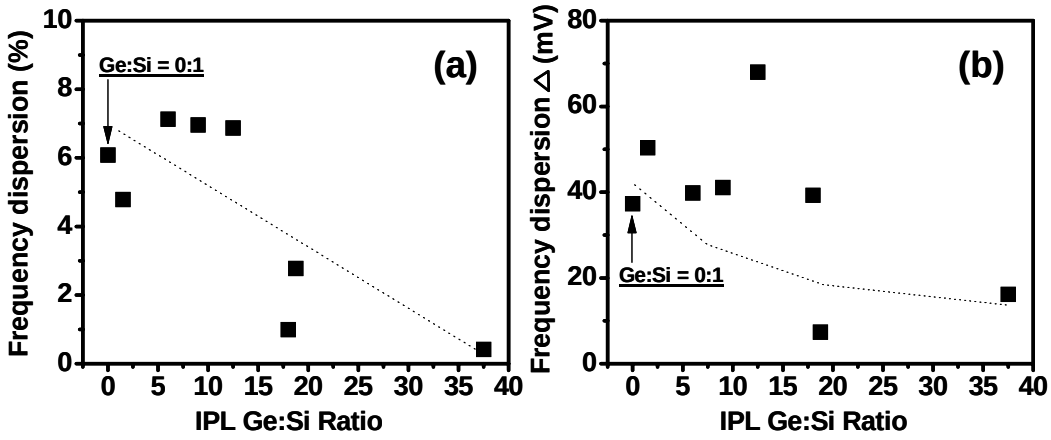

Figure 2.66 (a) Frequency dispersion (%) between 10KHz and 1MHz at 2.5V on n-type GaAs versus Ge:Si ratio in IPL (b) frequency dispersion (ΔmV) between 10KHz and 1MHz at flat band voltage on n-type GaAs versus Ge:Si ratio in IPL

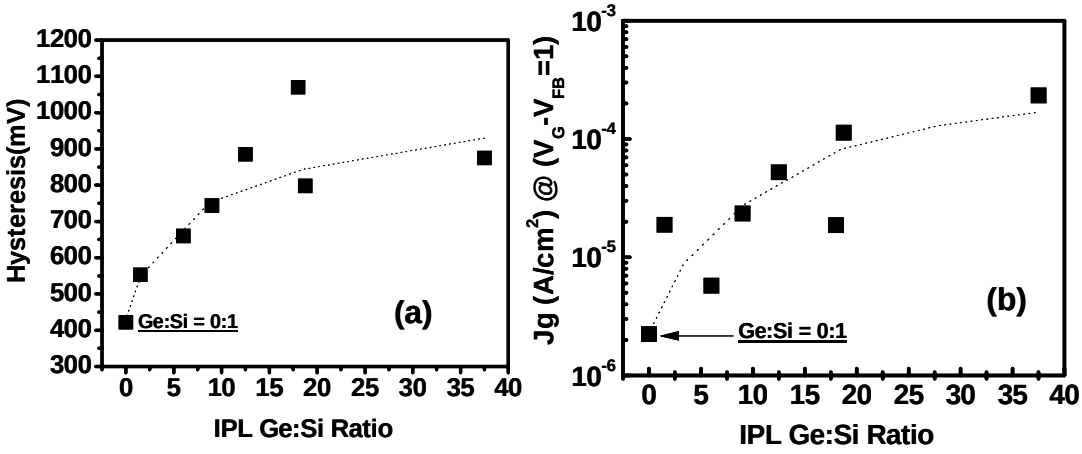

Figure 2.67. (a) Hysteresis versus Ge:Si ratio in IPL (b) Leakage current density Jg (A/cm2) at |Vg-VFB| = 1 versus Ge:Si ratio in IPL

The variation of frequency dispersion for Ge-rich IPL is also larger possibly because the deposition rate is higher than Si deposition. With appropriate thickness of SiGe IPL with optimum PDA condition, low frequency dispersion (< 5%) can be obtained. Leakage current also can be changed with different Ge:Si ratio (Fig. 2.67b). Ge-rich IPL shows slightly higher leakage current (~10^{-4} A/cm^2) than Si-rich IPL (~10^{-5} A/cm^2).

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Chapter 3: MOSCAP's and MOSFET's on InGaAs Channel Materials with Si Interface Passivation Layer

3.1 METAL GATE HfO_2 MOS STRUCTURES ON $In_{0.2}Ga_{0.8}As$ SUBSTRATE WITH VARYING SI INTERFACE PASSIVATION LAYER AND PDA CONDITION

3.1.1 Motivation

We have investigated the GaAs MOSFET using Si interface passivation layer (IPL) and HfO_2 as gete dielectric. In this work, we have investigated $In_{0.2}Ga_{0.8}As$ MOSCAP using the same oxide of HfO_2 as gate insulator with Si IPL. The advantages of high electron mobility of InGaAs have long been recognized, and many efforts to fabricate MOS transistors have been pursued. Both depletion- and enhancement-mode metal insulator field effect transistors (MISFET's) have been demonstrated, and the direct couple field effect logic (DCFL) based ring oscillators were also reported [1], [2]. However, the devices still showed current drifting, hysteresis, and negative threshold voltage for intended enhancement-mode device due to traps existing in the dielectrics and surface converting during the implant dopant activation annealing process. The key challenge for InGaAs-based MOSFETs is also the lack of high-quality, thermodynamically stable insulators that passivate the interface states and prevents Fermi level pinning at InGaAs-gate dielectric interface. Several groups have suggested improvements in the interface quality associated with the deposition of a thin silicon interlayer [3], [4] onto the as-grown InGaAs surface. In this paper, we present $In_{0.2}Ga_{0.8}As$ MOSCAP using the same oxide of HfO_2 as gate insulator with Si IPL using

physical vapor deposition (PVD) sputtering system. We studied the electrical characteristics of TaN/HfO_2/GaAs MOS capacitors with Si IPL under various PDA (post-deposition anneal) condition and various Si deposition temperature/time using MBE grown $In_{0.2}Ga_{0.8}As$ substrate.

3.1.2 Experiments

MOS capacitors were fabricated on MBE grown n-type InGaAs wafer doped with Si. A cross-sectional view of the MOSCAP is shown in Fig. 3.1.

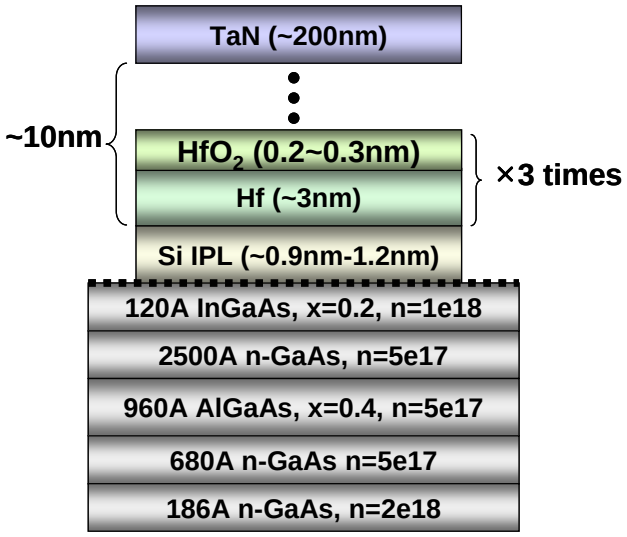

Figure 3.1. A cross-sectional view of the n-$In_{0.2}Ga_{0.8}As$ MOSCAP structure

The surface oxides were removed with a HCl and buffered oxide enchant (BOE) clean followed by $(NH_4)_2S$ dip, resulting in a clean S-passivated GaAs surface. Then Si IPL was deposited by RF sputtering of Si in Ar ambient at 400°C. PVD HfO_2 films were deposited using the modulation technique, followed by post-deposition anneal (PDA) at

600°C in N_2 (O_2 5%) ambient. The thickness of Si IPL layer varied from ~8Å (1min deposition time) to ~24Å (3min) measured by elipsometer and transmission electron microscope (TEM) images [5] and the physical thickness of HfO_2 layer was ~ 100Å. PVD TaN was used as gate electrode. After gate patterning using reactive ion etching (RIE) based on CF_4 gas, low-resistance ohmic contact was formed by using AuGe/Ni/Au alloy on the backside of the wafer [6]. The samples were then annealed at 450°C for 30sec in nitrogen. Electrical characterization was performed on MOS capacitors. EOT values were extracted from C-V characteristics.

3.1.3 Results and Discussion

After Hf deposition following by PDA, X-ray photoelectron spectroscopy (XPS) was measured. XPS showed that with 500°C and 600°C 1min PDA, Si was partially oxidized, and after 600°C 3min PDA, the Si IPL was oxidized to SiO_2 (Fig. 3.2a).

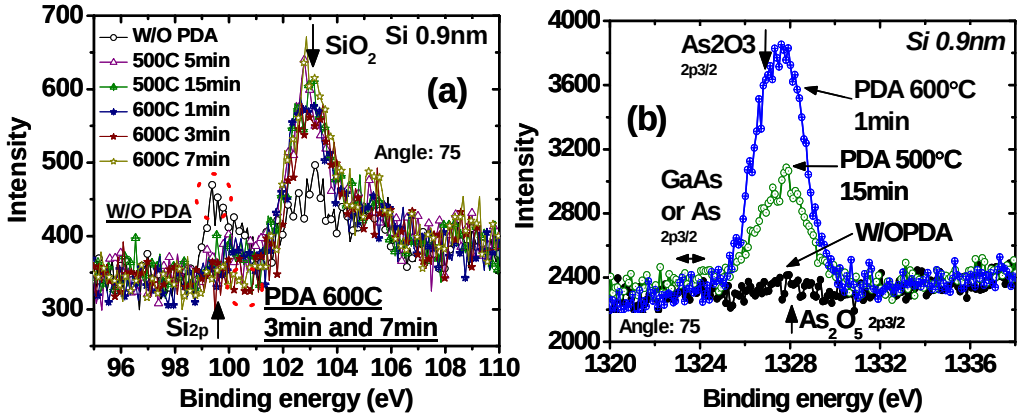

Figure 3.2. XPS spectra of the Si 2p (a) and As 2p for 90sec (~0.9nm) Si IPL thickness with different PDA time

While the As-O bonds were observed after anneal, no other distinguishable bonds were observed, in particular Ga 2p spectra was not detectable, and In 3d remained unchanged with different annealing condition..

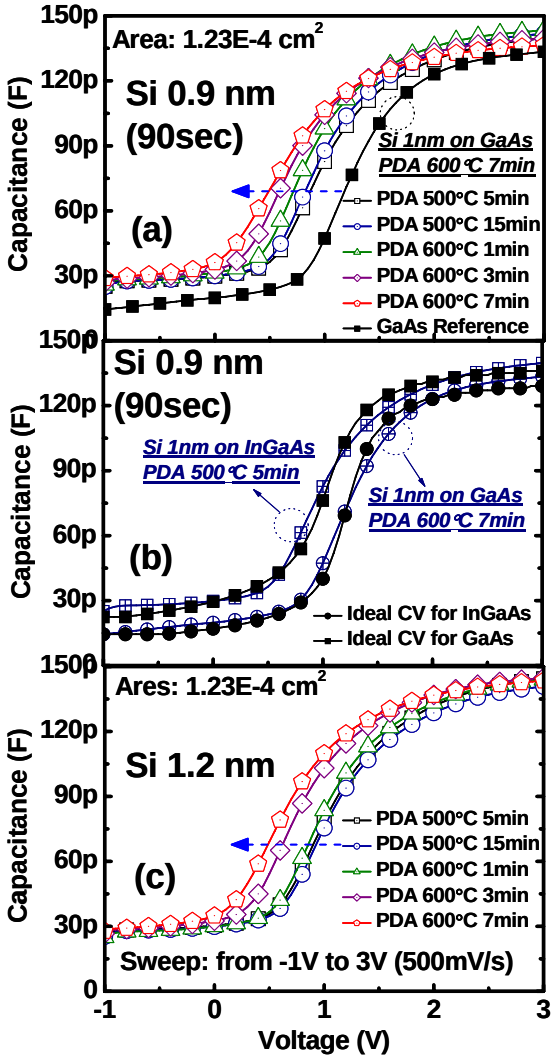

Figure 3.3. 1MHz CVs for (a) 90sec (~0.9nm) (b) comparison with ideal CV for InGaAs with 5min PDA at 500°C and GaAs with 7min PDA at 600°C, and (c) 120sec (~1.2nm) Si IPL with different PDA time

As shown in Fig. 3.2b, As_2O_3 was obtained through the PDA and the PDA above 600°C was shown that As_2O_3 intensity was much higher than As_2O_3 intensity with 500°C PDA. Fig. 3.3. show C-V characteristics with 90sec and 120sec Si IPL and different PDA condition. C-V characteristics of TaN/HfO_2/Si IPL/InGaAs/GaAs MOSCAP show similar behavior as those on GaAs-only substrate even though the depletion region might extend throughout the InGaAs layer and into GaAs substrate. As increase the PDA temperature and time, flat band voltage shift negative direction (Fig.3.4a) [7].

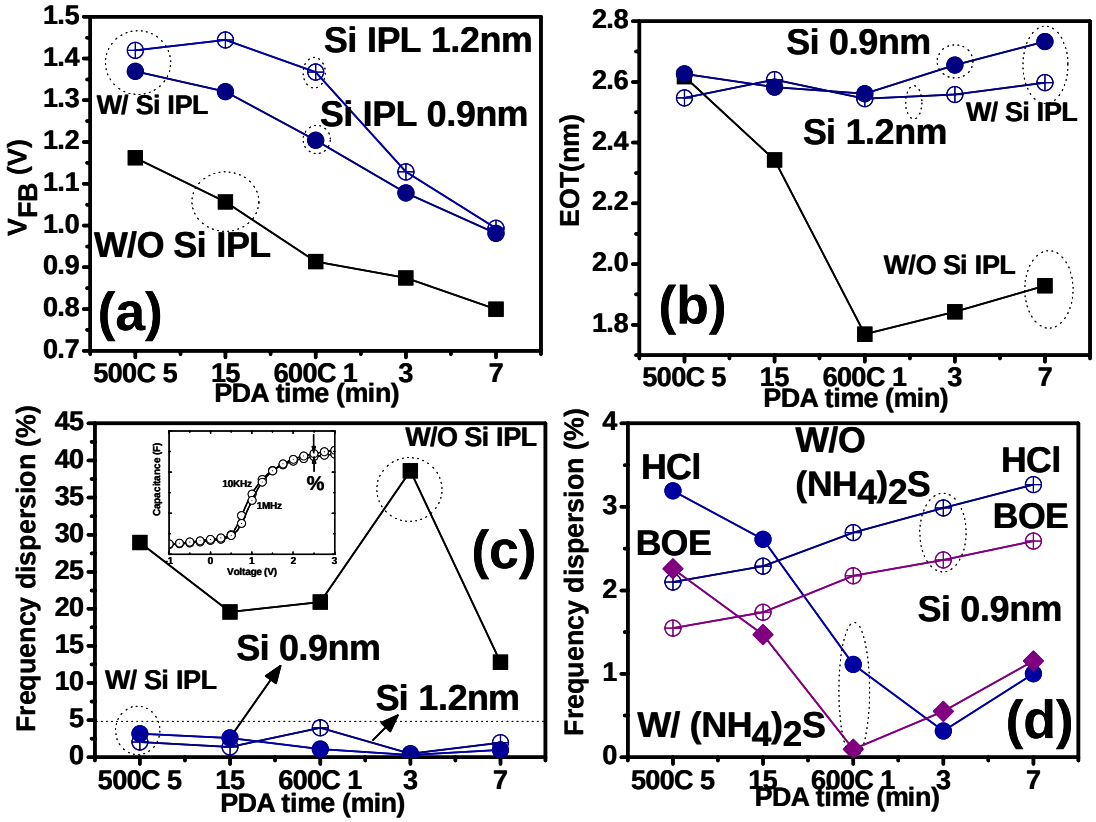

Figure 3.4. (a) V_{fb} shift, (b) EOT, (c) Frequency-dispersion (%), and frequency-dispersion (%) with different chemical cleaning methods as a function of PDA time (500°C 5min, 500°C 15min , 600°C 1min, 600°C 3min, and 600°C 7min)

The slopes of the flat band voltage shift for with Si IPL and without Si IPL structure are similar to each other. The results suggest that flat band voltage shift was more affected by the As-O defect (i.e. charge traps) than Si oxidation (Fig. 3.2). Ideal C-V [8] and experimental C-V are shown in Fig. 3.3b for InGaAs and GaAs reference samples. In general, varying Si deposition time still resulted in similar EOT values (Fig. 3.4b). Thin amorphous Si IPL between HfO_2 and $In_{0.2}Ga_{0.8}As$ substrate did not significantly contribute EOT change after PDA. EOT was mostly related to HfO_2 thickness. With increasing PDA time, negligible increase in SiO_2 thickness was observed. As_2O_3 (Fig. 3.2) and Si possibly behave as defects. Thus As_2O_3 and SiO_2 contributed to minimal change to EOT. Even though EOT is thinner for samples w/o Si IPL layer, C-V has severe leakage, hysteresis and frequency-dispersion. Fig. 3.4c and Fig. 3.4d summarize the frequency-dispersion characteristics (% definition of $(C_{10KHz}-C_{1MHz})/C_{1MHz}\times 100$ [%] at 2.5V is defined in Fig. 3.4c) versus PDA time with different Si IPL deposition condition. With appropriate thickness of Si IPL and PDA condition, reduced frequency-dispersion (< 5%) can be obtained. In contrast, without Si IPL, frequency-dispersion was around 15~40%. Si IPL was more effective to improve interface quality than different surface cleaning (Fig. 3.4d). Before Si deposition, InGaAs surface was cleaned by BOE or HCl with or without $(NH_4)_2S$ dip. In general, BOE cleaning resulted in slightly lower frequency-dispersion than HCl cleaning. As increased PDA temperature, $(NH_4)_2S$ dip resulted in a more stable interface between Si and InGaAs surface due to sulfide passivation (Fig 3.4d). Thus, the frequency-dispersion remained low even with higher PDA temperature and time.

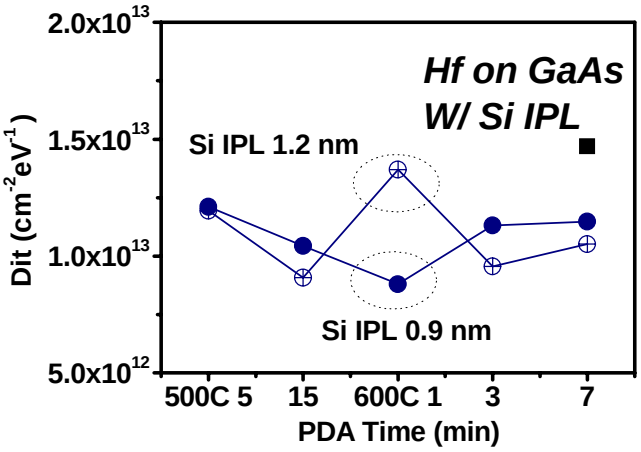

Figure 3.5. D_{it} as a function of PDA time with different Si IPL thickness and reference D_{it} of the same structure on GaAs substrate

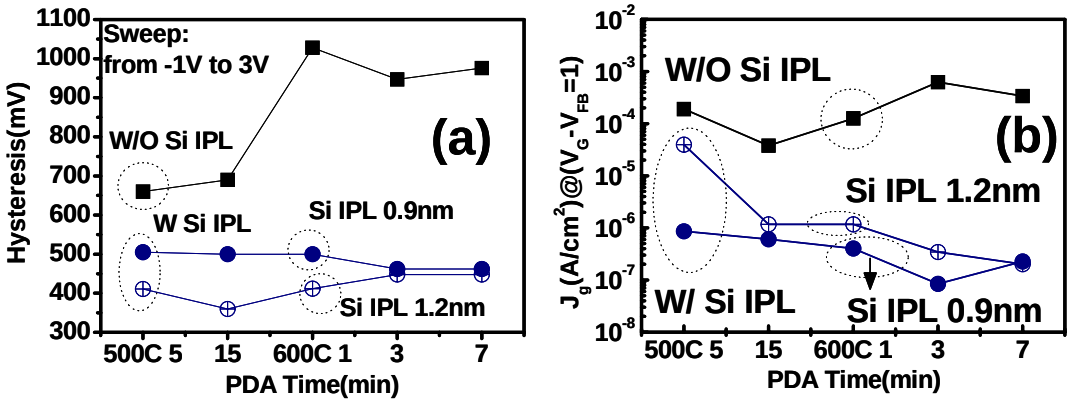

Figure 3.6. (a) Hysteresis for 1MHz CVs (sweep rate: 500mV/sec) and (b) Leakage current as a function of PDA time with different Si IPL thickness

Si deposition time of 90 second (~0.9 nm) with 7min PDA time resulted in ~10E13 D_{it} value which was similar to GaAs based structure using conductance method at V_{fb}-0.3V for each samples (Fig. 3.5). V_{fb} changed with different PDA condition (Fig. 3.3). However, D_{it} values remained relatively unchanged (Fig. 3.5). Thus V_{fb} shifts are

believed to be related to charge trapping in the gate stack, while D_{it} values are related to the interface quality. Si IPL led to lower hysteresis and leakage current (Fig. 3.6).

3.2 Hydrogen Incorporation of Metal Gate HfO_2 MOS Structures on $In_{0.2}Ga_{0.8}As$ Substrate with Si Interface Passivation Layer

Some experimental and theoretical investigations have been undertaken to understand the incorporation behavior of hydrogen into semiconductors, especially in Si and GaAs. In this work, we have investigated hydrogen incorporation effects for $In_{0.2}Ga_{0.8}As$ MOSCAP using the same oxide of HfO_2 as gate insulator with Si IPL and H_2 annealing at 500°C for 30min. A cross-sectional view of the MOSCAP is shown in Fig. 3.1. Electrical characterization was performed on MOS capacitors before and after H_2 annealing. Typical C-V characteristics of $TaN/HfO_2/Si/In_{0.2}Ga_{0.8}As$ as function of frequency and different PDA condition after H_2 annealing for 1.2nm Si IPL are shown in Fig 3.7.

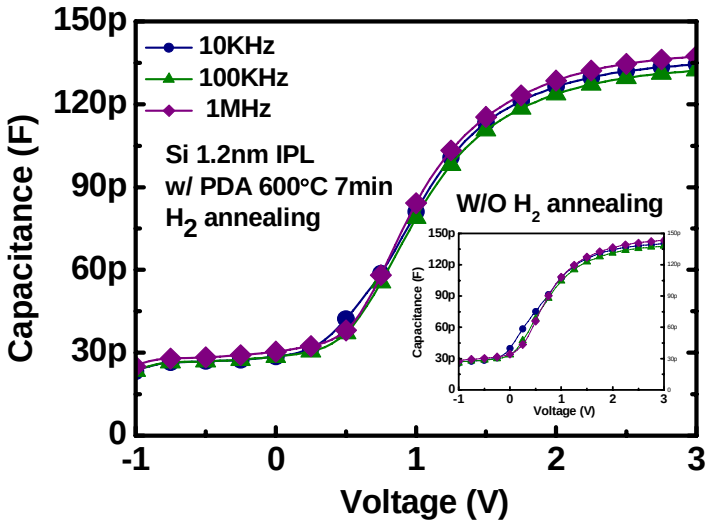

Fig. 3.7. Frequency dispersion for 120sec (~1.2nm) Si IPL with different PDA time

With increasing PDA temperature and time, flat band voltage shift negative direction however, after H_2 annealing, flat band voltage for all PDA samples shift positive direction with H_2 incorporation (Fig. 3.8). The slopes of the flat band voltage shift for with Si IPL and without Si IPL structure are similar to each other. The results suggest that flat band voltage shift was more affected by interfacial InGaAs oxide than Si oxidation and one of the clear contributions was As oxide (Fig. 3.2a) and hydrogen incorporation compensated the As oxide contributions.

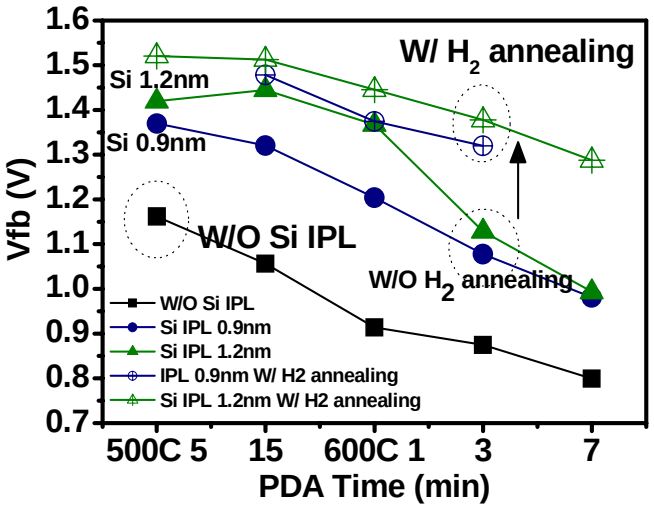

Figure 3.8. Flat band voltage shift as a function of PDA time

Fig. 3.9 summarize the frequency dispersion characteristics (% and ΔmV are defined in Fig. 3.7) versus PDA time with different Si IPL deposition condition and hydrogen incorporation. In general, hydrogen incorporation resulted in slightly lower frequency dispersion (% and ΔmV). In contrast, without Si IPL, frequency dispersion was around 15~40%.

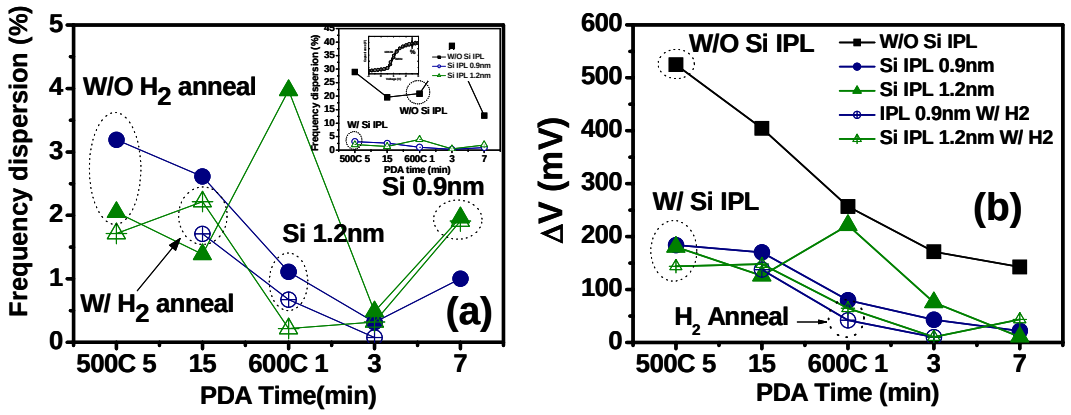

Figure 3.9. (a) Frequency dispersion (%) (b) Frequency dispersion (ΔmV) as a function of PDA time with different Si IPL thickness.

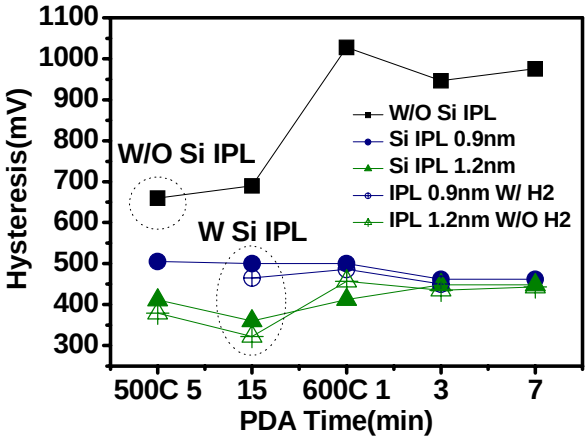

Figure 3.10. Hysteresis as a function of PDA time with different Si IPL thickness and H_2 annealing

Hydrogen incorporation resulted in similar hysteresis (mV) and EOT values (Fig. 3.10 and 3.11a). Thin amorphous Si IPL between HfO_2 and $In_{0.2}Ga_{0.8}As$ substrate with hydrogen incorporation did not significantly contribute to hysteresis characteristics which are more significantly affected by bulk HfO_2 than interface and to EOT change.

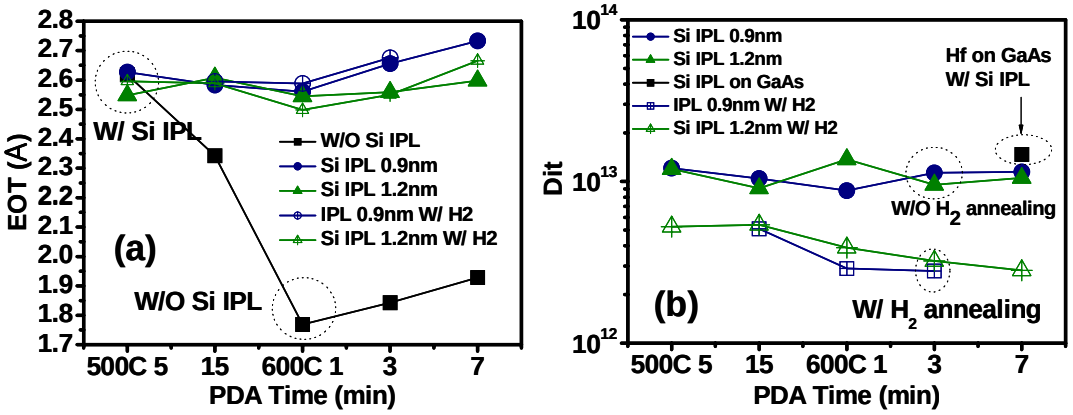

Figure 3.11. (a) EOT (b) D_{it} as a function of PDA time with different Si IPL thickness with H_2 annealing.

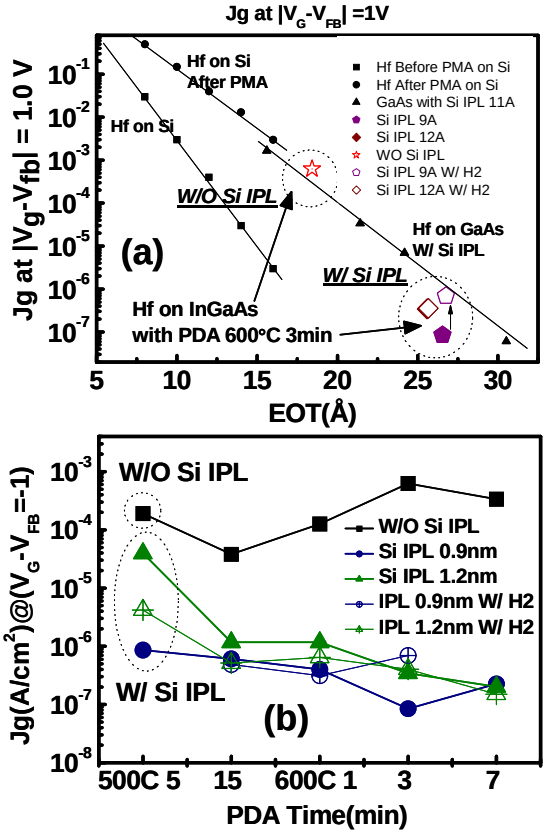

Figure 3.12. (a) Jg versus EOT for H_2 annealing samples (b) Leakage current as a function of PDA time with different Si IPL thickness.

Even though EOT is thinner for sample w/o Si IPL layer, the MOSCAPs exhibit high leakage, hysteresis and frequency dispersion. Si deposition time of 90 second (~0.9 nm) with 7min PDA time resulted in ~10^{13} D_{it} value which was similar to GaAs based structure using conductance method (Fig. 3.11b). Hydrogen incorporation samples resulted in lower D_{it} value ~2.8×10^{12} (~4 times less than W/O H_2 annealing). Si IPL with hydrogen incorporation led to similar leakage current (Fig. 3.12) which was less than the same structure with GaAs substrate.

3.3 METAL GATE – HfO_2 METAL-OXIDE-SEMICONDUCTOR (MOS) STRUCTURES ON HIGH-INDIUM-CONTENT $In_{0.53}Ga_{0.47}As$ SUBSTRATE USING PHYSICAL VAPOR DEPOSITION

The ternary alloy $In_{0.53}Ga_{0.47}As$ lattice matched to InP substrates is a promising material system for electronic and long wave length optical communication application. This material has a large ΓL inter-valley separation, high low-field electron mobility and saturation velocity. These characteristics should lead to devices with a high cutoff frequency and switching speed. Despite all the advantages of the InGaAs material system, the Schottky gate characteristics on InGaAs are very poor and metal semiconductor field effect transistors (MESFET's) can not be realized. Through the years, a variety of techniques such as plasma oxidation, silicon dioxide, silicon nitride, atomic layer deposition (ALD) Al_2O_3 and an epitaxial Si interface layer with different passivation techniques have been used to passivate the InGaAs surface to form the MISFET structure for better gate characteristics [9]–[18].

In this chapter, we present metal-oxide-semiconductor capacitor (MOSCAP) using the same oxide of HfO_2 by PVD as gate insulator without Si IPL but on high-indium-content $In_{0.53}Ga_{0.47}As$ channel. We report the electrical characteristics of $TaN/HfO_2/In_{0.53}Ga_{0.47}As$ MOS capacitors under various PDA (post-deposition anneal) condition and various indium content on $In_{0.53}Ga_{0.47}As$ substrate. MOS capacitors were fabricated on molecular beam epitaxy (MBE) grown n-type $In_{0.53}Ga_{0.47}As$ wafers doped with Si on n-type InP substrate. A cross-sectional view of the MOSCAP is shown in Fig. 3.13.

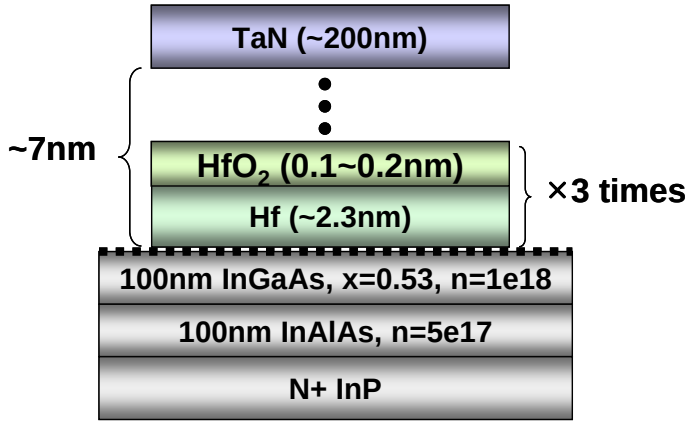

Figure 3.13. A cross-sectional view of the n-$In_{0.53}Ga_{0.47}As$ MOSCAP structure

The surface oxides were removed with a buffered-xide-etch (BOE) clean followed by $(NH_4)_2S$ dip, resulting in a clean S-passivated $In_{0.53}Ga_{0.47}As$ surface. A cross-sectional transmission electron microscopy (TEM) image of the gate stack is presented in Figure 3.14 (a) and (b). The interface between HfO_2 and GaAs surface was degraded severely after PDA of 600°C 3min (Fig. 3.14a). However, the interface between HfO_2 and $In_{0.53}Ga_{0.47}As$ surface had no distinct interface layer (IL) and without any degradation (Fig. 3.14b). After Hf deposition following by PDA, X-ray photoelectron spectroscopy

(XPS) was measured. XPS showed that as increased PDA time at 600ºC, Ga_2O_3 and As_2O_3 peak from reference (minimum line of each XPS intensity) on GaAs were much higher than on $In_{0.53}Ga_{0.47}As$ (Fig. 3.15a).

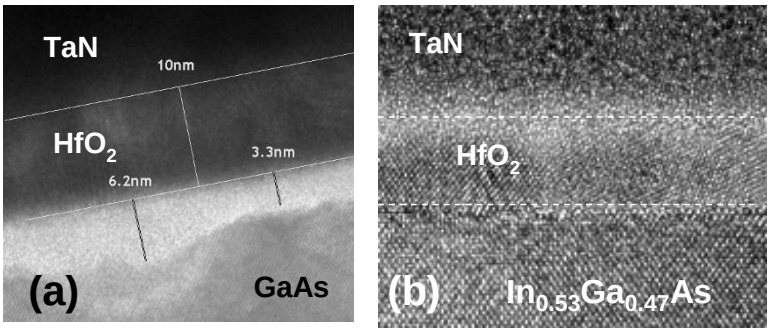

Figure 3.14. A cross-sectional transmission electron microscopy (TEM) image of the gate stack on (a) GaAs (b) $In_{0.53}Ga_{0.47}As$ with PDA of 600ºC 3min

After Hf deposition following by PDA, X-ray photoelectron spectroscopy (XPS) was measured. XPS showed that as increased PDA time at 600ºC, Ga_2O_3 and As_2O_3 peak from reference (minimum line of each XPS intensity) on GaAs were much higher than on $In_{0.53}Ga_{0.47}As$ (Fig. 3.15a).

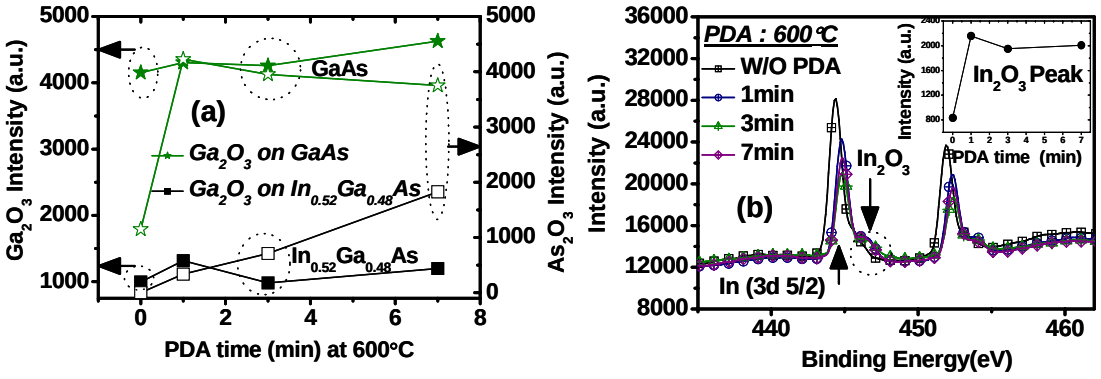

Figure 3.15. (a) XPS spectra: peak value of the Ga_2O_3 (2p 3/2) and As_2O_3 (2p 3/2) from reference with different PDA time (min) on GaAs and $In_{0.53}Ga_{0.47}As$ (b) XPS spectra of the In_2O_3 (3d 5/2) with different PDA time (min) on $In_{0.53}Ga_{0.47}As$. Inset shows In_2O_3 (3d 5/2) peak value from the reference with different PDA time

The variation for Ga_2O_3 peak between before and after PDA was small for both GaAs and $In_{0.53}Ga_{0.47}As$ samples. However, for high-indium-content $In_{0.53}Ga_{0.47}As$, Ga_2O_3 and As_2O_3 peaks were suppressed possibly due to indium or indium oxide (Fig. 3.15b). The frequency dispersion on accumulation capacitance is another important issue for high-k dielectrics on III-V and the trend of frequency dispersion has been correlated with the interface state density [19]. Fig. 3.16a summarizes the frequency dispersion characteristics (% definition of $(C_{1KHz}-C_{1MHz})/C_{1MHz}$ 100 [%] at 2.5 V is defined in inset of Fig. 3.16a) versus PDA time with different indium content substrate.

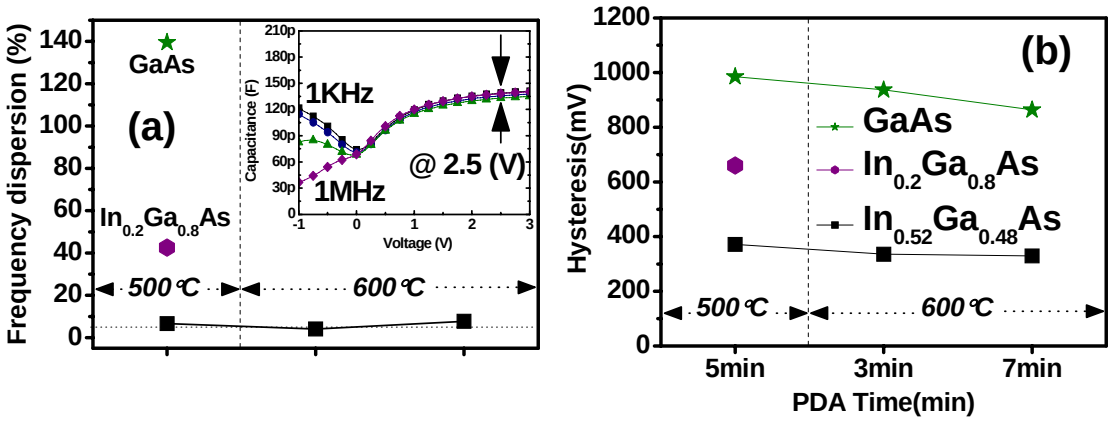

Figure 3.16. (a) Comparison of frequency dispersion on substrates with different indium content (b) Hysteresis for 1MHz CVs (sweep rate: 500mV/sec) versus PDA time with different substrate

The frequency dispersion could be as large as 140% for GaAs MOSCAPs in the frequency ranging from 1 kHz to 1 MHz. This implies high interface trap densities. Frequency dispersion (%) of MOSCAPs on $In_{0.53}Ga_{0.47}As$ show significantly smaller % in comparison to low indium content $In_{0.53}Ga_{0.47}As$ and GaAs with different PDA condition

(Fig 3.16a). Fig. 3.16b shows the effects of indium-content on hysteresis behavior of MOSCAPs with different PDA condition obtained from bidirectional high frequency CV measurements at 1MHz (sweep rate 500 mV/sec with sweep range from -1V to 3V). Hysteresis was measured between third and fourth sweep at each $V_{FB.}$ Hysteresis also shows similar trend as frequency dispersion in Fig 3.16a. $In_{0.53}Ga_{0.47}As$ samples show lower hysteresis (ΔmV) compared to $In_{0.2}Ga_{0.8}As$ and GaAs with various PDA conditions. EOT of samples is shown as a function of oxide physical thickness in Fig. 3.17a in which PDA of 500ºC 5 min samples exhibit slightly smaller EOTs as compared to PDA of 600ºC 1 min samples. The linear dependence of EOT on the physical thickness of HfO_2 give dielectric constant of HfO_2 around 23-25 with K_{sio2}=3.9. Fig. 3.17b illustrates the leakage current density (J_g) at $V_g = V_{fb}$+1 V versus EOT. Leakage current was reduced (to ~7.5×10^{-3} A/cm^2) for 3.0nm thickness of high-k dielectric on N-type $In_{0.53}Ga_{0.47}As$ wafer. High-indium-content $In_{0.53}Ga_{0.47}As$ led to lower leakage current compare to low indium content $In_{0.2}Ga_{0.8}As$ and GaAs.

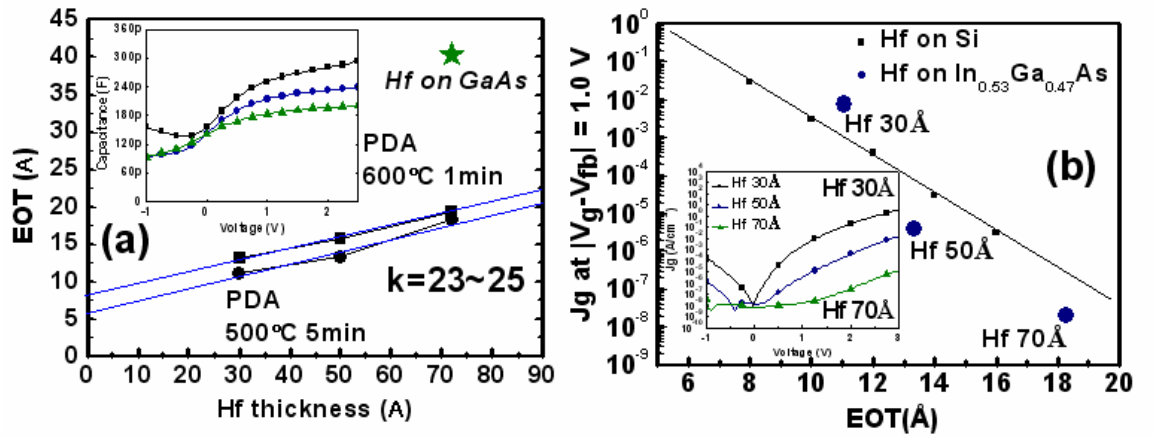

Figure 3.17 (a) equivalent oxide thickness (EOT) versus oxide (HfO_2) physical thickness with different PDA condition (b) leakage current density (Jg) versus EOT (Å) at V_{fb} + 1 [V] with $In_{0.53}Ga_{0.47}As$

3.4 METAL GATE – HfO_2 METAL-OXIDE-SEMICONDUCTOR (MOS) STRUCTURES ON HIGH-INDIUM-CONTENT $In_{0.53}Ga_{0.47}As$ SUBSTRATE USING PHYSICAL VAPOR DEPOSITION

In this chapter, we presents the electrical characteristics of TaN/HfO_2/$In_{0.53}Ga_{0.47}As$ MOS capacitors under various PDA (post-deposition anneal) condition and self-aligned n-channel MOS transistor with high temperature PMA on high-indium-content $In_{0.53}Ga_{0.47}As$ channel substrate with and without Si IPL.

MOS capacitors were fabricated on molecular beam epitaxy (MBE) grown n-type (1×10^{18} /cm^3) $In_{0.53}Ga_{0.47}As$ wafers doped with Si on n-type InP substrate. A cross-sectional view of the n-$In_{0.53}Ga_{0.47}As$ MOSCAP structure without Si IPL and with Si IPL (~1.5 nm) is shown in Fig. 3.18.

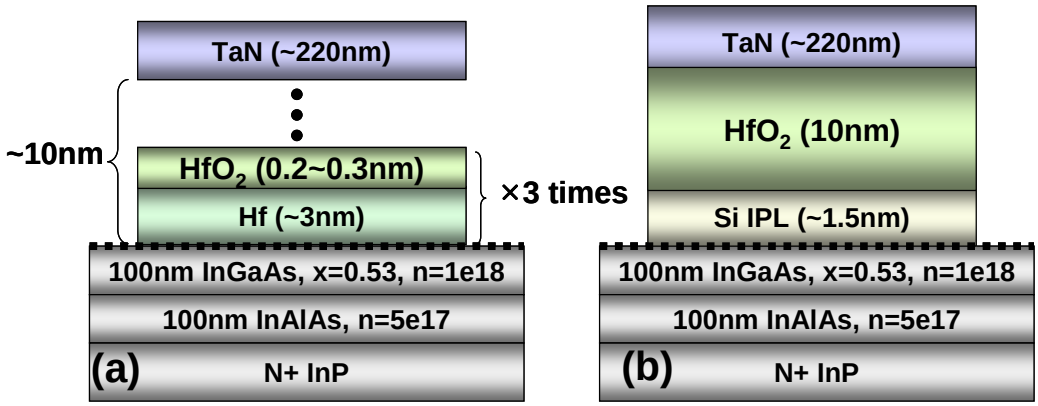

Figure 3.18. A cross-sectional view of the n-$In_{0.53}Ga_{0.47}As$ MOSCAP structure (a) without Si IPL and (b) with Si IPL (~1.2 nm)

For the purpose of improving the interface quality as in the case of GaAs, Si IPL was used for capacitors and transistor structures (Fig. 3.18b). However, contrary to the case of GaAs, the interface between HfO_2 and $In_{0.53}Ga_{0.47}As$ surface show no distinct interface layer (IL) or any degradation even without IPL, as shown in a cross-sectional

high resolution transmission electron microscopy (HRTEM) image of the gate stack with PDA 3 min at 600 ºC (Fig. 3.19a). The frequency dispersion on accumulation capacitance is an important issue for high-k dielectrics on III-V and the magnitude of frequency dispersion has been correlated with the interface state density.

Fig. 3.19(c) shows the frequency dispersion characteristics for sample with Si IPL 1.5 nm (Si deposition time 80sec) and PDA 3 min at 600 ºC (same sample as in Fig. 3.19b). The definition of % is C_{1KHz}-C_{1MHz})/C_{1MHz}×100 [%] at 2.5 V. Frequency dispersion (%) with Si IPL 1.5 nm and PDA 3 min at 600 ºC shows very small value (0.5 %). This implies low interface trap densities. Electron energy loss spectroscopy (EELS) shows that n-$In_{0.53}Ga_{0.47}As$ surface was oxidized due to oxidation process after Hf deposition (Fig. 3.19d and 3.19e). Frequency dispersion (%) of MOSCAPs on $In_{0.53}Ga_{0.47}As$ with Si IPL shows smaller % in comparison to that without Si IPL with different PDA condition (Fig 3.20a). Frequency dispersion for the samples 1.2 nm of Si IPL and 1.5 nm Si IPL shows similar value for each different PDA condition and for PMA of 750 ºC 12sec.

EOT of samples is shown as a function of PDA in Fig. 3.20b in which samples with Si IPL exhibit larger (~1.0 nm) EOTs as compared to samples without Si IPL due to SiO_2 formation during PDA. In general, EOT differences between the samples with 1.2nm of Si IPL and 1.5nm of Si IPL are negligible. Unoxidized thin amorphous Si IPL between HfO_2/SiO_2 and $In_{0.53}Ga_{0.47}As$ substrate did not significantly contribute EOT change after PDA. EOT was mostly related to HfO_2 thickness and interface oxide including SiO_2. The EOT values were found to be fairly independent of PDA condition (Fig 3.20b).

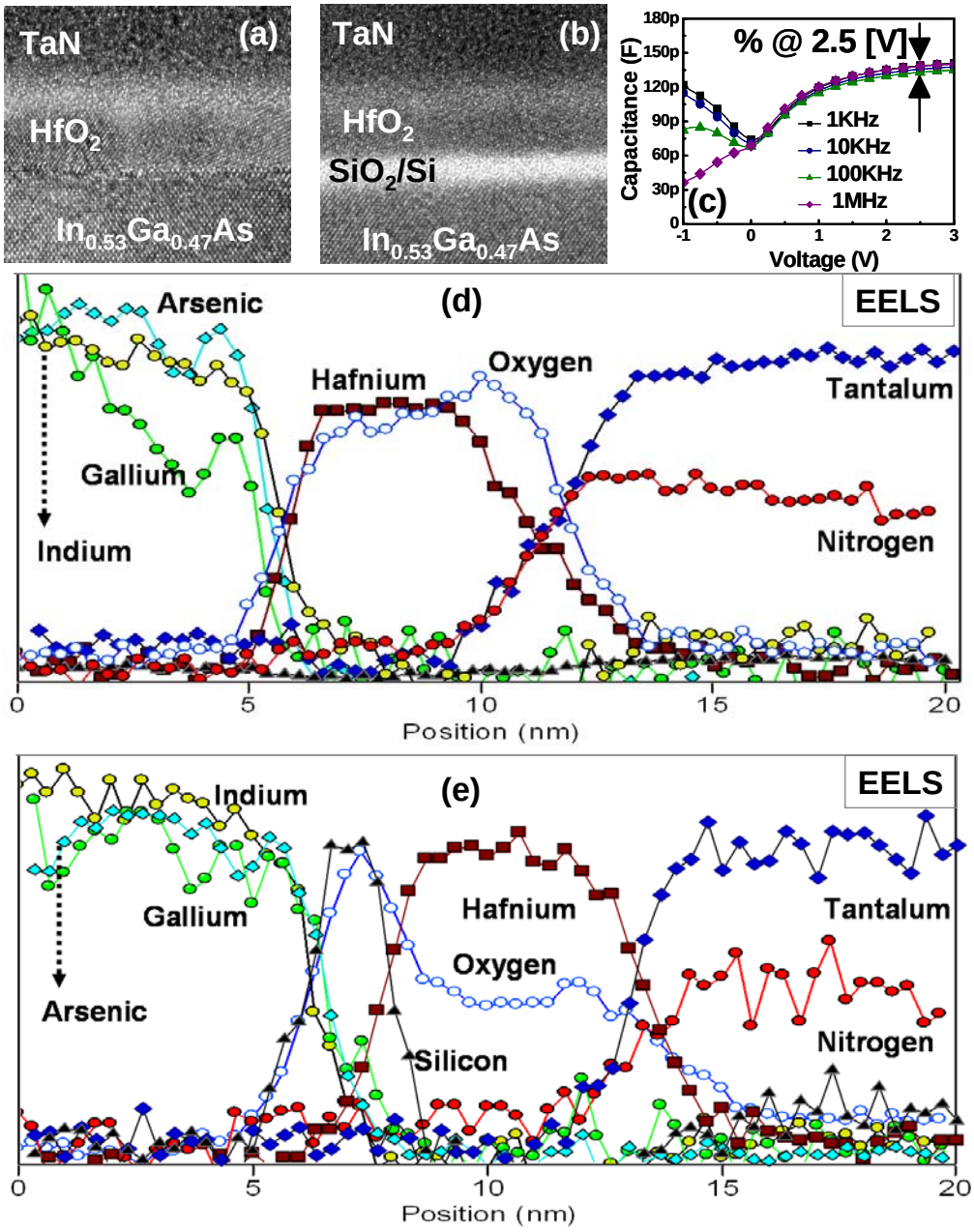

Figure 3.19. A cross-sectional high resolution transmission electron microscopy (HRTEM) image of the gate stack on $In_{0.53}Ga_{0.48}As$ with PDA of 600 ºC 3 min (a) without Si IPL (b) with Si IPL (~1.2 nm) (c) CV with different frequency for sample (b). (d) Electron energy loss spectroscopy (EELS) analysis on figure (a) image. (e) Electron energy loss spectroscopy (EELS) analysis on figure (b) image.

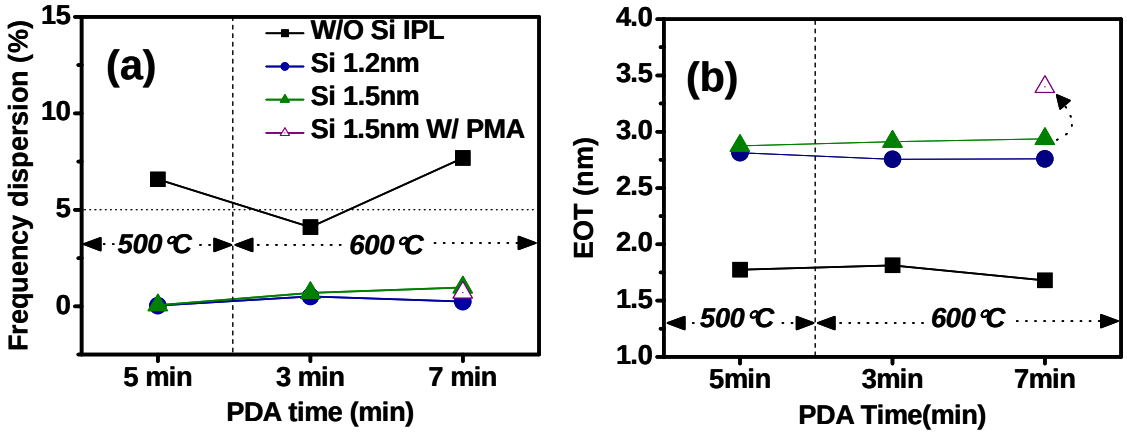

Figure 3.20. Comparison of (a) frequency dispersion (%) (b) EOT with different Si IPL thickness as a function of PDA time (500 °C 5 min, 600° C 3 min, and 600 °C 7 min) and PMA (750 °C 12 sec) for the sample with Si IPL 1.5 nm and PDA of 600 °C 3 min.

This suggests that the formation of SiO_2 and native oxide such as In_2O_3, Ga_2O_3 and As_2O_3 was suppressed. The EOT was increased by 0.45 nm after PMA of 750 ºC 12sec for the sample of Si IPL of 1.5 nm and PDA of 600 ºC 7 min. Fig. 3.21b shows the effects of Si IPL on hysteresis behavior of MOSCAPs with different PDA conditions obtained from bidirectional high frequency CV measurements at 1MHz (sweep rate 500 mV/sec with sweep range from -1 to 3 V).

Hysteresis was measured between third and fourth sweep at each $V_{FB.}$ Hysteresis also shows similar trend as frequency dispersion in Fig 3.21(a). It has been found that the hysteresis was reduced significantly using the Si IPL. In general, thicker Si IPL led to lower hysteresis (ΔmV). Hysteresis is believed to be due to charge trapping/detrapping between high-k layer and the substrate as the voltage is swept back and forth. Thus, a

thicker SiO_2 IPL layer could lead to larger distance between HfO_2 and GaAs substrate and thereby lower hysteresis. With PMA, hysteresis was reduced to 86 mV (Fig 3.21a).

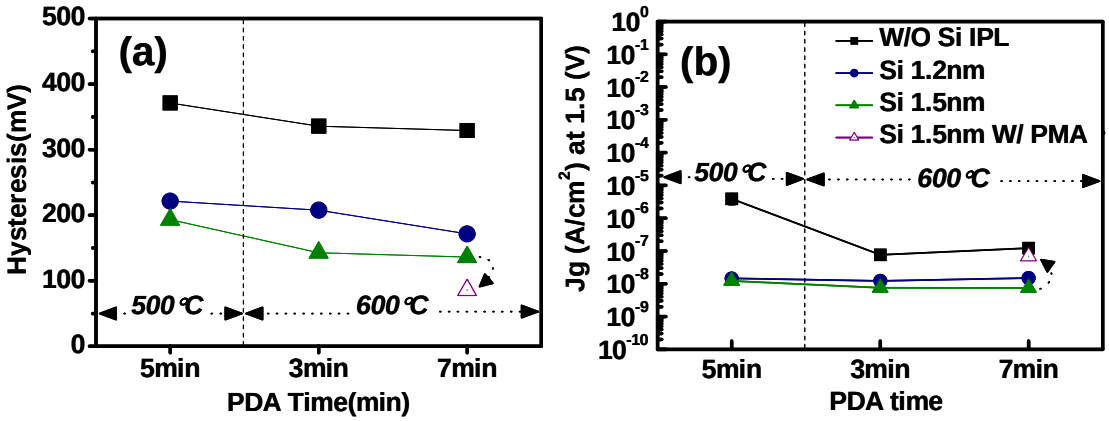

Figure 3.21. Comparison of (a) hysteresis (b) leakage current at 1.5 V with different Si IPL thickness as a function of PDA time (500 °C 5 min, 600° C 3 min, and 600 °C 7 min) and PMA (750 °C 12 sec) for the sample with Si IPL 1.5 nm and PDA of 600 °C 3 min.

Fig. 3.21b illustrates the leakage current density (J_g) as a function of PDA at V_g = 1.5 V. Leakage current was reduced (to ~7.4×10^{-9} A/cm^2) for 10.0nm thickness of high-k dielectric with 1.5 nm of Si IPL on N-type $In_{0.53}Ga_{0.47}As$ wafer. Leakage current was reduced by using the Si IPL. In general, longer PDA time, thicker Si IPL led to lower leakage current. With PMA, the leakage current was increased to 6.8×10^{-8} A/cm^2 from 7.4×10^{-9} A/cm^2.

We fabricated $In_{0.53}Ga_{0.47}As$ nMOSFETs employing the same gate stack using a ring-FET geometry consisting of an annular gate, in order to simplify the device isolation process. The schematic cross section and top view of n-MOSFET with Si passivation is shown in Fig. 3.22. Si IPL layer with thickness ~1.5 nm was deposited for transistor fabrication to prevent Fermi level pinning at the $In_{0.53}Ga_{0.47}As$-HfO_2 interface.

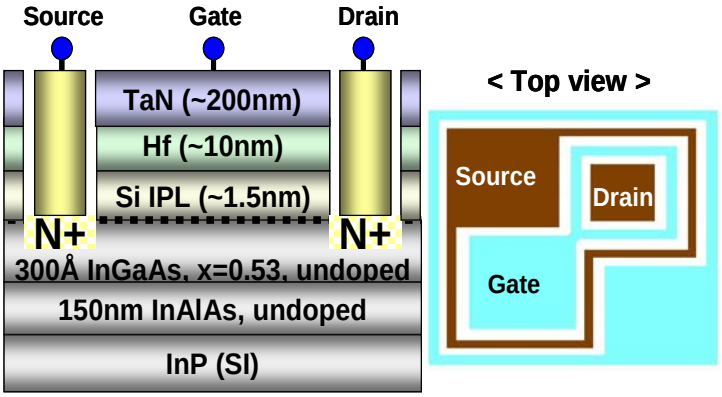

Figure 3.22. schematic cross section and top view of n-MOSFET with Si passivation 1.5 nm.

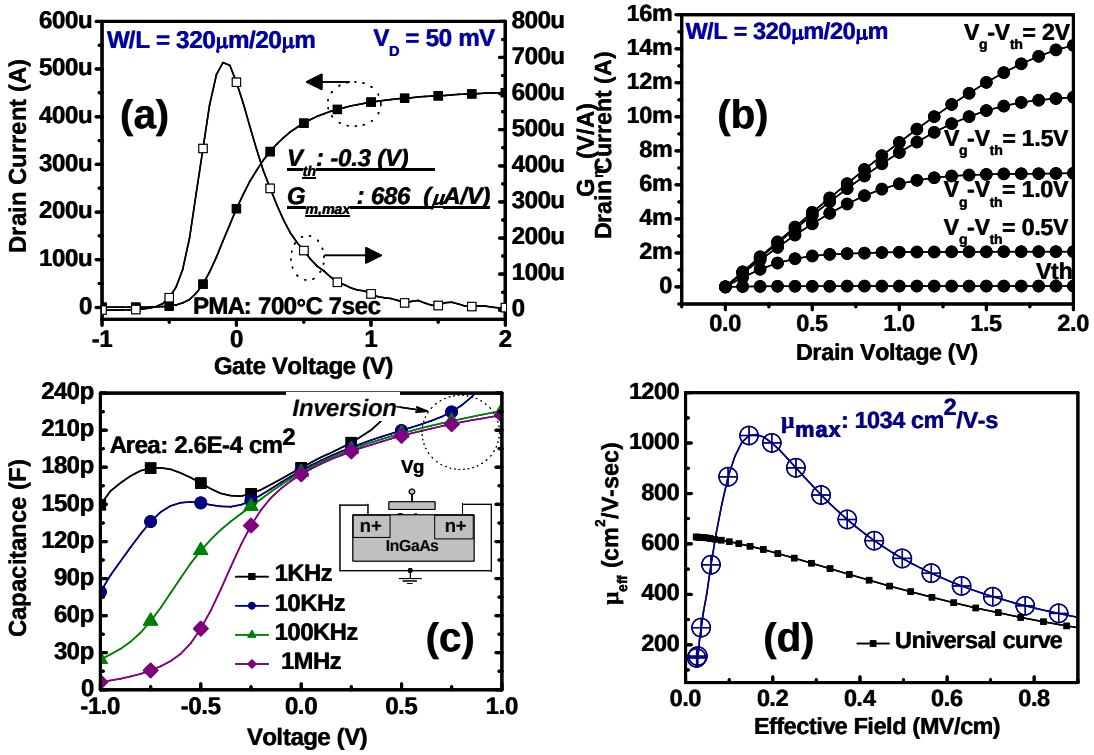

Figure 3.23. (a) I_d-V_g and G_m of n-MOSFET with Si passivation (W320 μm× L 20 μm) with peak G_m 686 (μA/V) and V_{th} -0.3 V. (b) I_d-V_d of n-MOSFET with Si passivation (W320 μm× L 20 μm). (c) frequency dispersion of n-MOSFET with Si 1.5 nm and PMA 700 °C 7 sec. (d) mobility of n-MOSFET with Si passivation (W320 μm× L 20 μm) from split CV and I_d-V_g curve (closed: mobility of universal curve on Si substrate).

Figure 3.23 (a) shows the transfer characteristics of an nMOSFET with a gate width of 320 μm and length of 20 μm. A threshold voltage of -0.3 V was extracted by linear extrapolation technique. A maximum transconductance (G_m) of 686 (μA/V) was obtained for the device at a drain voltage of 0.05 V. The output characteristics of the MOSFET device are illustrated in Fig. 3.23 (b) where a maximum drain current of 14.2 mA was obtained at a V_g-V_{th} of 2 V and V_d of 2 V. Figure 3.23 (c) shows split CV characteristics of the MOSFET, measured at different frequencies, showing a frequency dispersion behavior. The effective electron mobility (μ_{eff}) was evaluated for the same device from the I_d-V_g plot (measured at a drain voltage of 50 mV) and its corresponding split C-V (Fig 3.23d). Peak mobility of 1034 cm^2/V-s has been obtained.

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Chapter 4: MOSCAP's and MOSFET's on InP Channel Materials with Si Interface Passivation Layer

4.1 Self-aligned n-channel InP MOSFETs on undoped substrates using physical vapor deposition (PVD) HfO_2 and Silicon interface passivation layer

In this work, as an alternative of silicon substrate, Indium-phosphide (InP) has been studied. InP metal-oxide-semiconductor field-effect transistor (MOSFETs) have important potential applications in high-frequency digital circuits, microwave power amplifiers, and monolithic optoelectronics circuits. High electron mobility (5200 cm/V s) and high saturation velocity (2.5×10^7 cm/s) are the two key properties which make InP attractive for this application. The InP MOSFETs can be readily configured for enhancement-mode operation, thus allowing low-power dissipation to be achieved in digital circuits. As a result of the insulated gate, a large dynamic range for the circuit can be achieved leading to a larger logic swing and consequently better noise margins. The larger breakdown voltage, higher thermal conductivity, and lower ionization coefficient compared to GaAs make InP a better choice for microwave power generation. InP is expected to play an important role in optical fiber telecommunications since the long-wavelength optical devices use InP as the substrate.

Compared to GaAs, InP is far more suitable for MOSFET applications because the density of interface states near the conduction-band edge is small enough [1] provided that appropriate insulator formation condition is employed. A number of techniques have been used to fabricate these devices [2-6]. Early efforts also were directed at the

development of an InP MOS technology using anodic [3-4] and thermal [5-6] oxides as gate insulators. However, the use of such oxides was abandoned due to the low resistivity ($r \approx 10^{12}\,\Omega cm$) and large density of interface states near the midenergy gap (1-5~10^{11} cm^{-2} eV^{-1}). To date, the best results for an InP MOS structure have been achieved with deposited dielectric layers such as: SiO_2 using direct and indirect chemical vapor deposition (CVD) [7-9], pyro-lyticy [10-11] and photo-CVD [12-13] techniques and with many efforts to passivate the surface in order to "unpin" surface Fermi level have been pursued [14-25].

We have recently demonstrated effective passivation of GaAs, InGaAs using an amorphous Si IPL layer [26-29]. The minimum thickness of the Si layer preventing Fermi level pinning at GaAs-HfO_2 interface was found to be ~1.2 nm (PVD deposition time 60sec) for MOSCAP and 1.5nm (PVD deposition time 80sec) for MOSFET [29]. Previously, few papers reported InP MOSFET with poor transistor characteristics [30]. More recently MOSFET with atomic-layer-deposited (ALD) Al_2O_3 gate dielectric showed inversion-type enhancement-mode n-channel transistor performance [31]. In this paper, we present the material and electrical characteristics of TaN/HfO_2/InP self-aligned n-MOSFET with PVD Si IPL under various post deposition anneal (PDA) conditions. We also demonstrated N-channel high-k InP MOSFETs with good transistor behavior.

4.2 EXPERIMENTS

MOS capacitors were fabricated on n-type ($1\sim5\times10^{17}/cm^3$) InP (100) wafer doped with Si. A cross-sectional view of the MOSCAP structure is shown in Fig. 4.1(a) and 4.1(b).

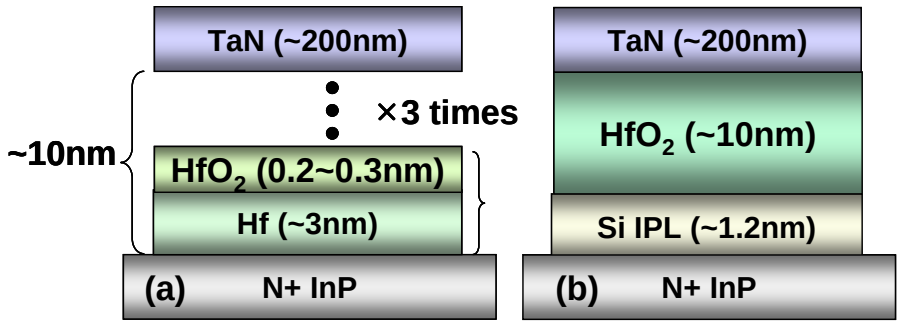

Figure 4.1. A cross-sectional view of the n-InP MOSCAP structure (a) without Si IPL and (b) with Si IPL

The surface oxides were etched with a buffered oxide etch (BOE) clean followed by $(NH_4)_2S$ dip, resulting in a clean S-passivated InP surface. Then PVD Si and HfO_2 (~10nm thick) films were deposited by DC magnetron sputtering of Hf in Ar ambient using the modulation technique, followed by rapid thermal annealing (RTA) reoxidation (400°C, 500°C, and 600°C, 3min) process in N_2 (O_2 5%) ambient. In the modulation deposition technique, thin hafnium layer (~3.0nm measured by ellipsometry) was first deposited and then, thin HfO_2 (2~3nm measured by ellipsometry) layer was deposited in Ar+O_2 ambient. At this step, O_2 was provided to make HfO_2 as a buffer between the Hf layers. Hf layer works as an oxidation barrier during HfO_2 deposition. During PDA, the three stacked layers of Hf+HfO_2 were oxidized into a single layer of HfO_2 (~10 nm) as measured by ellipsometry and transmission electron microscope (TEM) images. PVD TaN (2200Å) was used as gate electrode followed by reactive ion etch (RIE) in CF_4 gas

ambient. After ion implantation with Si for source and drain, a RTA of 650°C for 7sec was used for S/D activation. Low-resistance ohmic contact was formed by using evaporation of AuGe/Ni/Au alloy and lift-off process, for n-type. The samples were then annealed at 450°C for 30sec in nitrogen ambient. Capacitance-voltage (CV) curves and MOSFETs output characteristics were measured by HP 4194 LCR meter and HP 4156 semiconductor parameter analyzer respectively.

4.3 RESULTS AND DISCUSSION

Fig. 4.2 illustrates transmission electron microscopy (TEM) on the MOSCAP with 10nm HfO_2 with PDA of 600°C 3 min for the sample with and without Si IPL. Approximately 0.8nm of the interface layer (IL) was formed between HfO_2 and InP surface during 600°C 3 min PDA for sample without Si IPL (Fig. 4.2a). To improve the interface quality, Si IPL was used for capacitors and transistor structures (Fig. 4.2b, 4.2d). Electron energy loss spectroscopy (EELS) shows that InP surface was oxidized due to oxidation process after Hf deposition (Fig. 4.3). Most of oxygen signal near the substrate interface overlapped with indium signal while very small area of phosphorus signal overlapped with oxygen signal (Fig 4.2c). After Hf deposition following by PDA, X-ray photoelectron spectroscopy (XPS) was measured. XPS showed that with increasing PDA temperature, In_2O_3 spectra increased (Fig. 4.3a). On the other hand, samples with 1.2nm of Si IPL showed no appreciable changes in indium oxides spectra indicating a suppression of In_2O_3 formation (Fig. 4.3b).

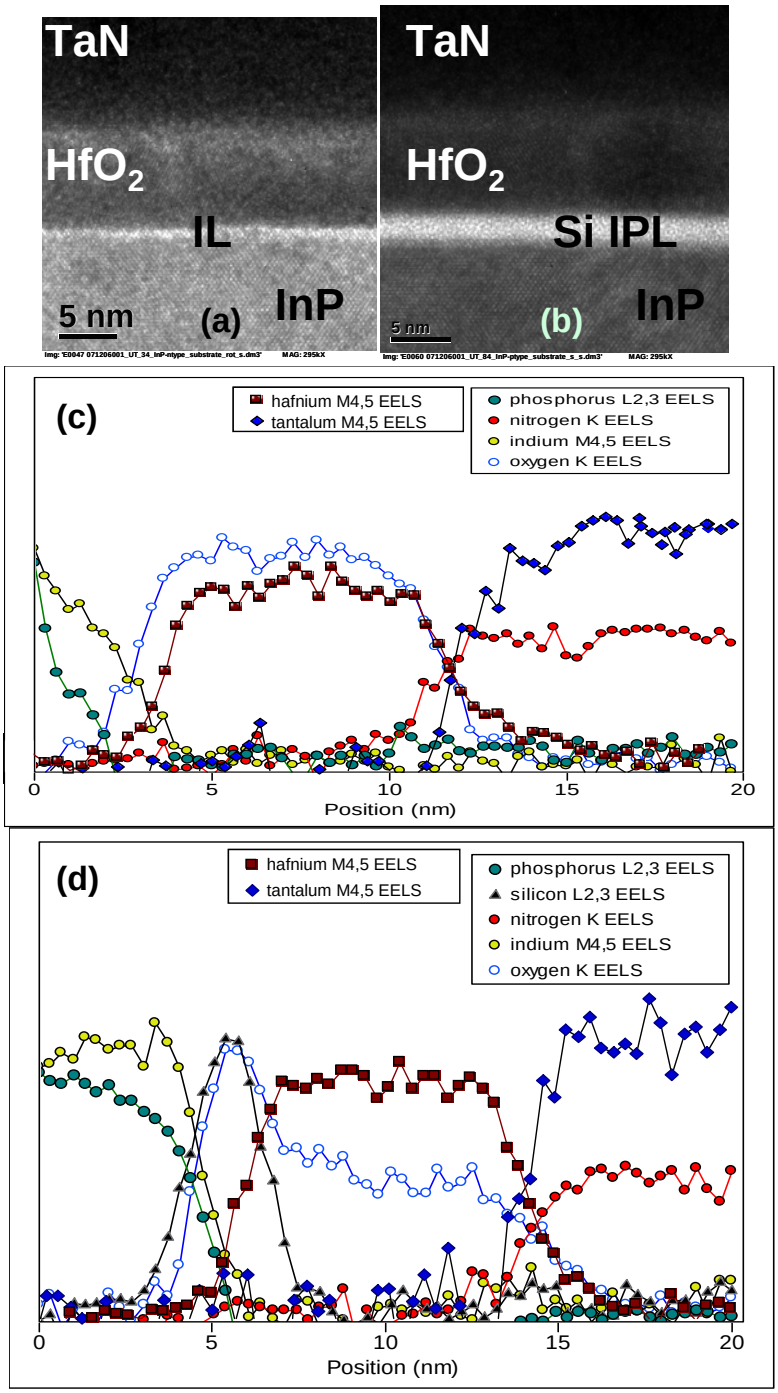

Figure 4.2. (a) A cross-sectional transmission electron microscopy (TEM) image of the gate stack on InP with ~0.8 nm of native oxide after PDA of 600ºC 3min (b) A cross-sectional transmission electron microscopy (TEM) image of the gate stack on InP with ~1.2 nm of Si IPL after PDA of 600ºC 3min (c) Electron energy loss spectroscopy (EELS) analysis on figure (a) image and (d) on figure (b) image.

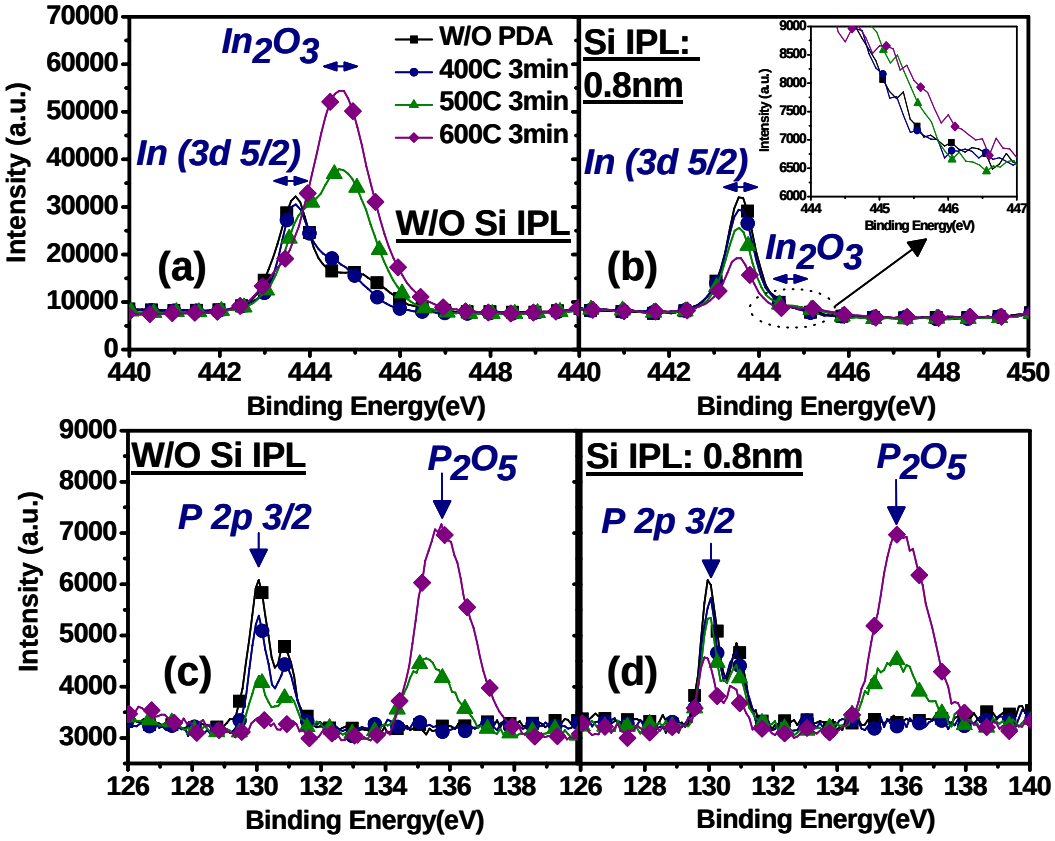

Figure 4.3. (a) XPS spectra of the In_2O_3 (3d 5/2) with different PDA temperature on InP. (b) with 1.2 nm of Si IPL. (c) XPS spectra of the P_2O_5 (2p 3/2) with different PDA temperature on InP. (d) with 1.2 nm of Si IPL.

The increasing PDA temperature drove the remaining phosphorus oxide increase but the peaks on the samples without Si IPL and with Si IPL show almost similar value for each different PDA condition (Fig 4.3c, 4.3d). XPS also show that Si was more oxidized with higher PDA temperature for samples with 60sec Si deposition time (1.2nm) (Fig 4.4a). In general, EOT differences between the samples with 1.2nm of Si IPL and 1.5nm of Si IPL are negligible (Fig. 4.4b). However, samples without Si IPL resulted in much thinner EOT thickness.

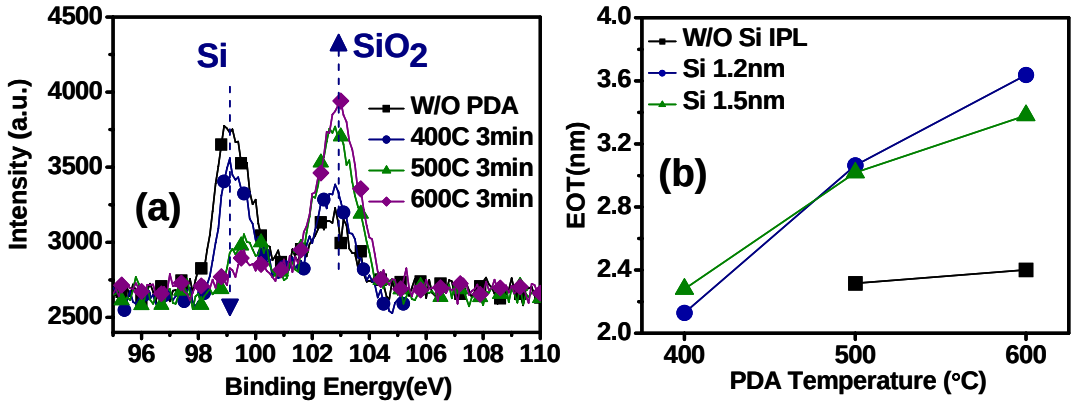

Figure 4.4. (a) XPS spectra of the Si (2p) with different PDA temperature on InP with 1.2nm of Si IPL. (b) Equivalent oxide thickness (EOT) versus different PDA temperature for 3min with 1.2nm and 1.5nm of Si IPL.

The thin amorphous Si IPL between HfO_2/SiO_2 and InP substrate did not significantly contribute EOT change after PDA. EOT was mostly related to HfO_2 thickness and interface oxide including SiO_2. With increasing PDA time, Si layer was changed to SiO_2 and increased EOT with formation of In_2O_3 and P_2O_5 (Fig. 4.4b). So In_2O_3, P_2O_5 and SiO_2 caused the change to EOT and the differences between samples without Si IPL and with Si IPL were mainly came from SiO_2 formation. Fig. 4.5a illustrates the leakage current density (J_g) at $V_g = V_{fb}+1$ [V]. Si IPL and higher temperature PDA led to lower leakage current (Fig. 4.5a). Leakage current was reduced (to ~9.7×10^{-9} A/cm^2) for 10 nm thickness of high-k dielectric with 1.5 nm of Si IPL and PDA of 500ºC 3min on N-type InP wafer. The frequency dispersion on accumulation capacitance is another important issue for high-k dielectrics on III-V and the trend of frequency dispersion has been correlated with the interface quality.

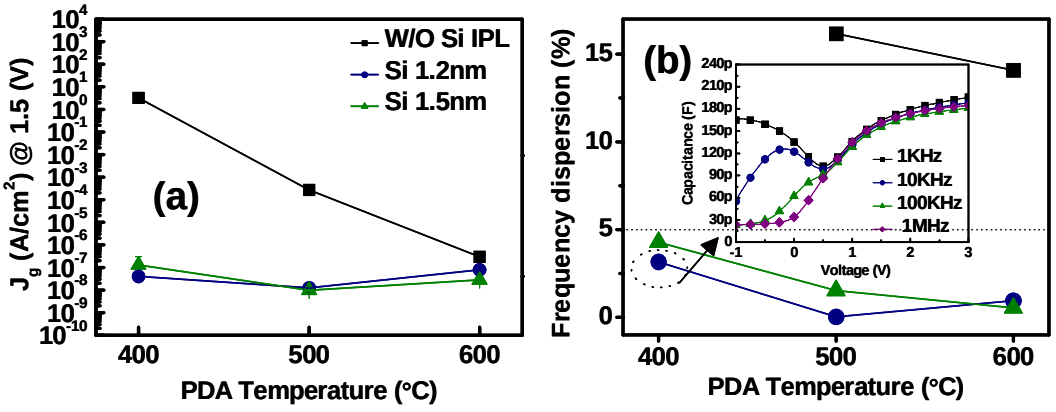

Figure 4.5. (a) Leakage current density (Jg [A/cm2]) at 1.5 [V] versus different PDA temperature for 3min with 1.2nm and 1.5nm of Si IPL. (b) Frequency dispersion (%) versus different PDA temperature for 3min with 1.2nm and 1.5nm of Si IPL and without Si IPL. Inset figure show CV with different frequency with 1.2nm of Si IPL after PDA of 400 ºC for 3min.

Fig. 4.5b summarize the frequency dispersion characteristics (% definition of $(C_{1KHz}-C_{1MHz})/C_{1MHz}\times100$ [%] at 2.5V) versus PDA temperature with different Si IPL deposition condition. With appropriate thickness of Si IPL and PDA condition, low frequency dispersion (< 5%) can be obtained. In contrast, without Si IPL, frequency dispersion was around 15%. This implies that ~0.8nm of native oxide (Fig 4.2a) might consist of high trap densities. The inset of Fig. 4.5b illustrates CV characteristics of the MOS capacitors, fabricated on n-type substrates with different frequencies for sample with 1.2nm of Si IPL and PDA of 400ºC for 3min. The capacitance increase in the inversion region is due to minority carrier generation in the substrate. We fabricated InP nMOSFETs employing the same gate stack using a ring-FET geometry consisting of an annular gate, in order to simplify the device isolation process. The schematic cross section and top view of n-MOSFET with Si passivation is shown in Fig. 4.6.

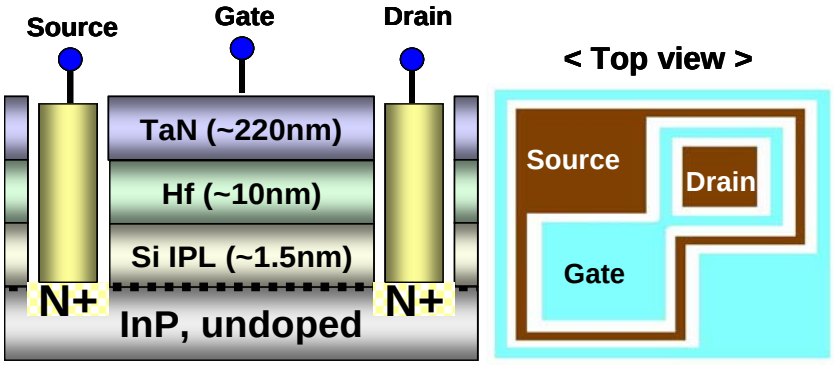

Figure 4.6. Schematic cross section and top view of n-MOSFET with Si passivation 1.5nm.

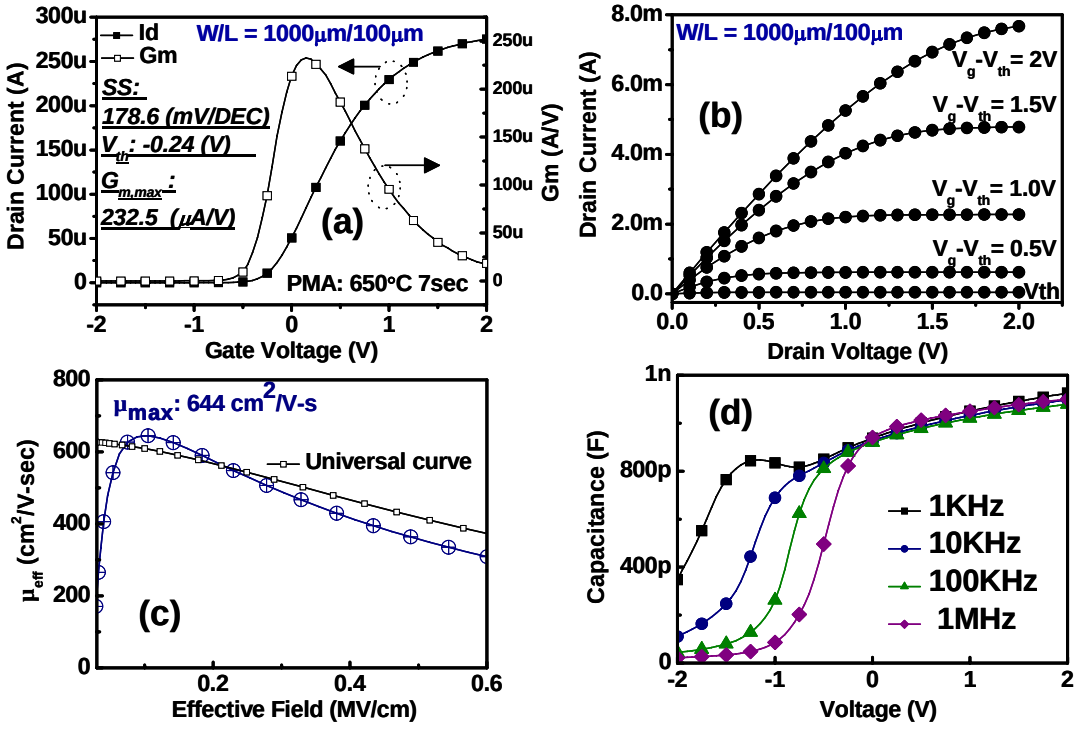

Figure 4.7. (a) I_d-V_g and G_m of n-MOSFET with Si passivation (W1000μm L 100μm) with peak G_m 232.5 (μA/V). (b) I_d-V_d of n-MOSFET with Si passivation (W1000μm L 100μm). (c) Mobility of n-MOSFET with Si passivation (W1000μm L 100μm) from split CV and I_d-V_g curve (d) frequency dispersion of n-MOSFET with Si 1.5nm and PMA 650°C 7sec.

Si IPL layer with thickness ~1.5 nm (PVD deposition time 80sec) was deposited for transistor fabrication to prevent Fermi level pinning at the InP-HfO_2 interface. Figure 4.7 (a) shows the transfer characteristics of an nMOSFET with a gate width of 1000μm and length of 100μm. A subthreshold slope (SS) of 178mV/dec were determined from the I_d-V_g plot. A threshold voltage of -0.24V was extracted by linear extrapolation technique. A maximum transconductance (G_m) of 232.5 (μA/V) was obtained for the device at a drain voltage of 0.05V. The output characteristics of the MOSFET device are illustrated in Fig. 4.7 (b) where a maximum drain current of 6.87mA was obtained at a V_g-V_{th} of 2V and V_d of 2V. The effective electron mobility (μ_{eff}) was evaluated for the same device from the I_d-V_g plot (measured at a drain voltage of 50mV) and its corresponding split C-V (Fig 4.7c). Fig. 4.7 (d) shows split CV characteristics of the MOSFET, measured at different frequencies, showing a frequency dispersion behavior. Peak mobility of 644 cm^2/V-s has been obtained.

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Chapter 5: Conclusions and Future Researches

5.1 SUMMARY OF RESEARCHES

In this Ph.D. dissertation, most gate dielectric researches were devoted to three major investigations based on understanding of electrical and material characteristics with some reliability, and process development for GaAs, InGaAs and InP. The first one is that the understanding of HfO_2 high-k dielectric material and its relationship with Si IPL (interfacial passivation layer) in terms of evaluation in MOS device characteristics. Here, the inserted Si IPL with HfO_2 high-k dielectric in GaAs has been studied. Si IPL with partially SiO_2 or Ge with HfO_2 on GaAs have found to play an important role to determine the electrical characteristics of MOSCAPs and MOSFETs.

Secondly, as another alternative substrate, characteristics on InGaAs with and without Si IPL and HfO_2 high-k dielectric MOSFET were investigated. For better electrical and material understanding, different substrates with varying substrate doping concentration were introduced. The electrical characteristics with dependency of frequency, flat band voltage shift with hydrogen annealing and material analysis provided insight of trapping in HfO_2 high-k dielectric and interface quality. In this work, the improvements of MOSFET characteristics such as output current, transconductance, channel mobility, etc., were especially emphasized with ultra-thin EOT regime (~ 10 Å) in order to overcome the drawback of HfO_2 on GaAs. Demonstration of NMOSFET on InGaAs with high-k dielectric can provide optimistic result near the future and possibility as alternative substrate to substitute conventional SiO_2 on Si substrate.

The third major research is that the process development of another alternative substrate with high-k gate dielectric material on InP for future scaled-down CMOS technology and applications in high-frequency digital circuits, microwave power amplifiers, and monolithic optoelectronics circuits. MOSFET characteristics with output current, transconductance, channel mobility, etc., were also emphasized. Using optimum thickness of the Si IPL preventing Fermi level pinning at InP-HfO_2 interface, ~1.2 nm (PVD deposition time 60sec) for MOSCAP and 1.5nm (PVD deposition time 80sec) for MOSFET, material and electrical characteristics of TaN/HfO_2/InP self-aligned InP n-MOSFET with PVD Si IPL under various post deposition anneal (PDA) conditions was studied with good transistor behavior.

5.2 SUGGESTIONS FOR FUTURE RESEARCHES

The remaining works for future researches based on this dissertation can be categorized as follows to continue and improve the related fields.

A. Further Scaling Issues

One of the major reasons to develop high-k on III-V transistor was that disadvantages of high-k dielectric with low channel mobility from scaling down. In order to keep sailing down for future technology node, the capacitance of gate dielectric needs to be increased. One approach is using higher-k dielectric material. The other is scale-down the physical thickness of dielectric. TiO_2/HfO_2 and Gd_2O_3/HfO_2 might provide the

way to approach of not only achieving possible low EOT, but also reducing the trapping of carrier by decreasing physical thickness of HfO_2. The room for this area needs to be focused on the development and optimization of structure in terms of fabrication process such as the thickness ratio of dielectric layers, PDA and PMA time, the uniformity of dielectric, etc. Also, it is strongly recommended that the understanding of charge effects in each layer of bi-layer structure dielectric, since these charges with different polarities can affect to electrical characteristics such as threshold voltage and channel mobility.

B. **Reliability of high-k on III-V**

The reliability is one of the major concerns with high-k dielectric for better evaluation. Specifications, mostly adapted from Si, issue need to be defined accurately.

1) Mobility

- How do we extract mobility accurately: using split CV, etc.
- Determination of key mobility scattering mechanism

2) TDDB or BTI test for high-k dielectric with bi-layer dielectric on III-V substrate

3) Electrical characterization with novel methods to determine intrinsic properties of the materials and develop model-based understanding of device performance.

4) Conform to EOT

– Jg specs for high-k/metal gate stack on Si

- Ideally CET less than 1nm at Jg of 10 amp/cm^2
- How to determine EOT with any Model

5) V_{th} $\pm$0.1 V of control high-k/Si with same EOT.

- Determine what influences V_{th}
- Is there fermi level pinning ?

- What is extent of V_{fb} and V_{th} tunability by changing work function of metals

- Determine effective WF of metals in this stack..

6) Density of interface traps (D_{it}) $\leq 5x10^{10}$ # / cm^2eV

- How to determine accurately?

- AC conductance, Charge pumping, 1/f noise, DC measurements etc ..

- How can one measure N_{it}/D_{it} for buried channels?

7) Determine nature of traps causing hysteresis related to bulk/interface mechanism and nanostructure (amorphous/crystalline)

- comparison to optimized high-k/Si.

C. Multi-metal dielectric application for III-V

For development of multi-metal dielectric, the thermodynamic stability of material provided information of possible reactions with III-V substrate. This is the main reason for adopting a bi-layer structure on Si substrate. For future research, it is interesting if the multi-metal dielectric will be deposited on III-V such as GaAs, InGaAs, or InP. The bi-layer structure might not be necessary for these substrates. Also, effect of charges in dielectric to substrate expected to be different, resulted in possible change of electrical characteristics such as mobility, hysteresis, stress incorporated measurement, etc.

D. Metal gate electrodes application for high-k on III-V

Multi-metal dielectric MOSFET could be suitable for different metal gate electrode with small or large work function. The evaluation of candidate materials for n-

and p-MOSFET compatible metal gate electrode with multi-metal dielectric is recommended for future work with developing multi-dielectric or alternative high-k dielectrics.

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Vita

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